A summary of IntSim+3D's models

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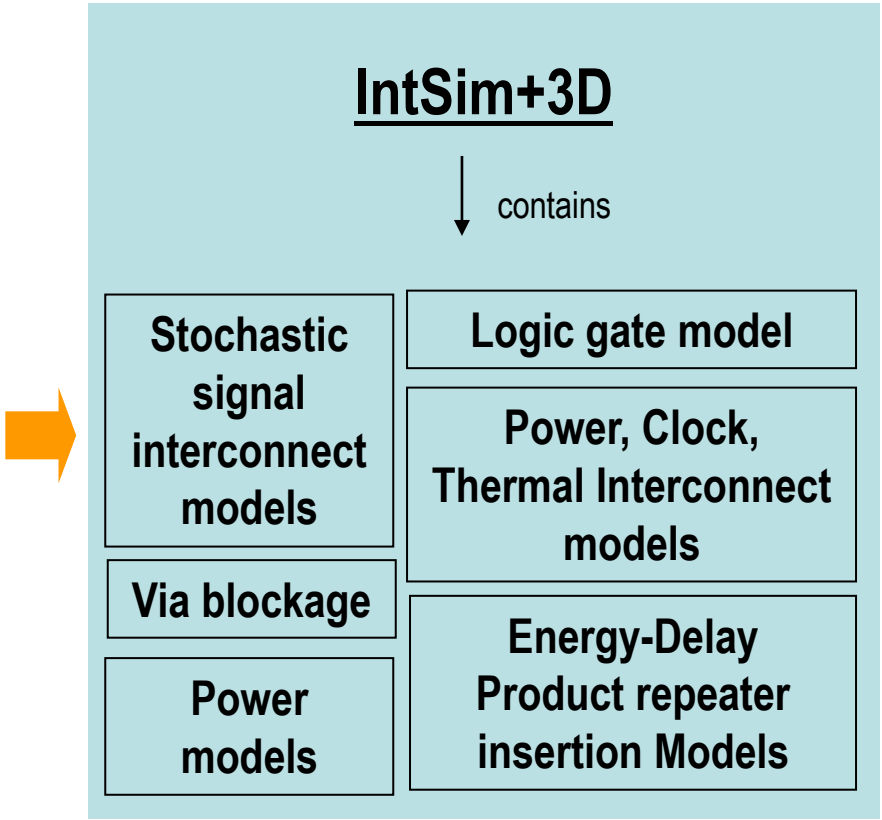
IntSim+3D: A Simulator for 2D or 3D-ICs

Inputs

- Gate count
- Die area
- Frequency
- Rent's parameters
- Number of strata

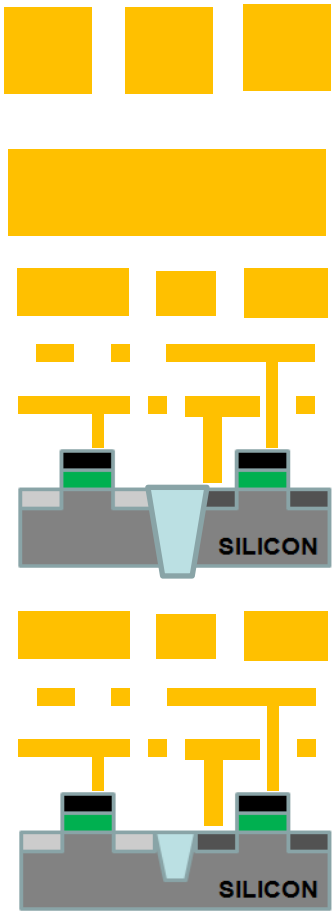
  (1 if 2D, >=2 for 3D)



Outputs

- Chip power
- Metal level count
- Wire pitches

IntSim+3D: Uses a novel algorithm to combine many models



Global interconnect levels

Shared among all strata

Model → [D. C. Sekar, J. D. Meindl, et al., IITC 2006]

Local and semi-global interconnect levels

Each stratum has its own

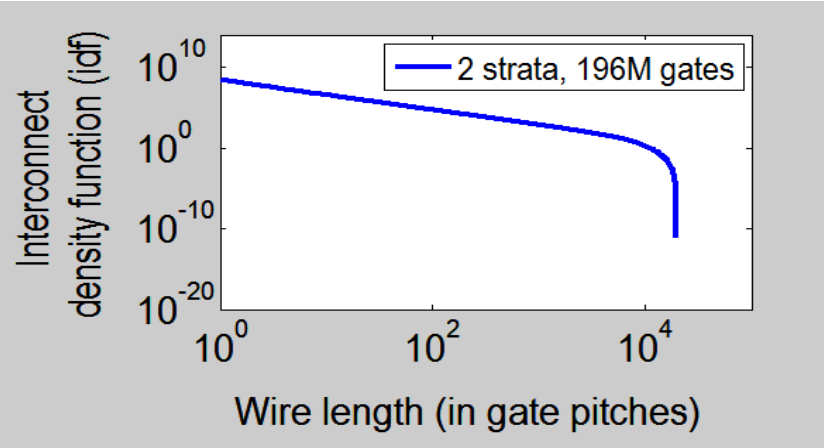
Models → [PhD dissertations of A. Rahman (MIT), R. Venkatesan, D. Sekar, J. Davis, R. Sarvari (all Georgia Tech students in Prof. Jim Meindl's group)]

Logic gates

Critical path model developed by K. Bowman (Georgia Tech)

Stochastic Signal Wire Length Distribution Model

Number of wires of length l = Function(Number of gates, die size, strata, feature size, Rent's constants)



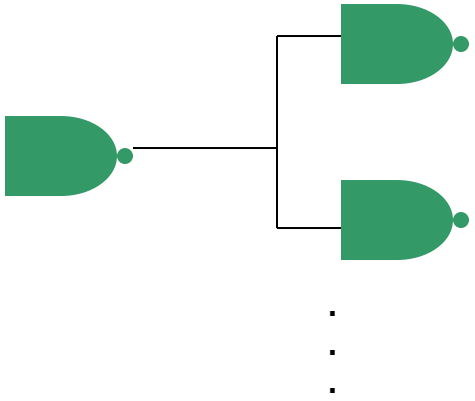
Number of wires of length between l and l+dl = idf(l) dl

- **Models from J. Davis, A. Rahman, J. Meindl, R. Reif, et al.**
  [A. Rahman, PhD Thesis, MIT 2001] [J. Davis, PhD Thesis, Georgia Tech, 1999]
- **2D model → fits experimental data reasonably well [J. Davis, PhD Thesis, GT, 1999]**
  3D model → same methodology

Logic gate model

Logic gates:

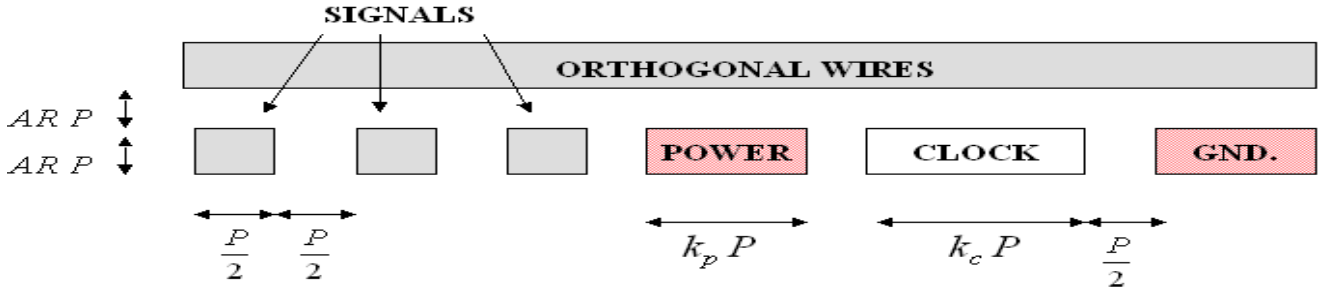
Two input NAND gates with average wire length, fan-out user defined



$$t_d = L_d 0.7 \frac{R_{NAND}}{W} \left(f.o.C_{NAND} W + f.o.\chi c L_{avg} \right)$$

Find W for a certain performance target

Global interconnect model



$$P = Max.\left[\begin{array}{l} 2.\left(k_p + 0.5\right).N_{power\_pads}.\rho.\dfrac{I_T.d_{pad\_to\_pad}{}^2}{\pi.e_{router}.A.AR.k_p.V_{IR}}.\ln\left(\dfrac{0.65.d_{pad\_to\_pad}}{l_{pad}}\right), \\ \dfrac{D}{2}\sqrt{\dfrac{c_{clock}\rho}{AR\cdot k_c R_o C_o}}.\dfrac{1}{\dfrac{\beta_0}{fR_oC_o}-11}\left(\sqrt{72.6+\dfrac{4.4\beta_0}{fR_oC_o}}+11\right) \end{array}\right]$$

Global wire pitch obtained based on two conditions:

(1) Signal bandwidth maximized with power grid IR drop requirement being reached

(2) Wire pitch big enough to drive a clock H tree of a certain length

Results match well with commercial processors [D. C. Sekar, et al., IITC 2006]

Local and semi-global interconnect model

Condition 1:

Wiring area available = Wiring needed for routing the stochastic wiring distribution

$$e_w 2A = \chi P \sqrt{\frac{A}{N_{sockets}}} \int_{l_{min}}^{l_{max}} li(l)dl$$

Condition 2:

RC delay of longest signal wire in each wiring pair = fraction of clock period

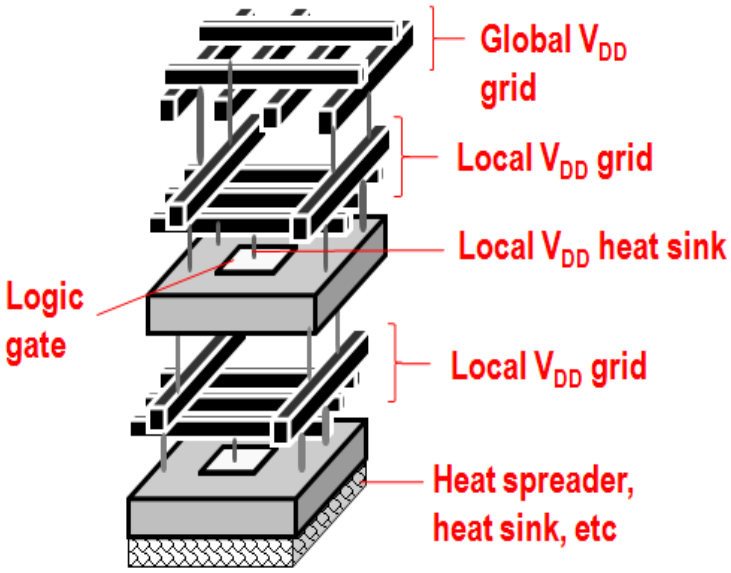
For wires with repeaters, new Energy-Delay Product repeater insertion model used

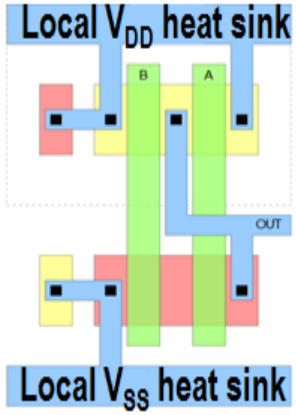
Condition 3:

Wire efficiency (e_w) = 1 – fraction of wiring area lost to power wiring, via blockage

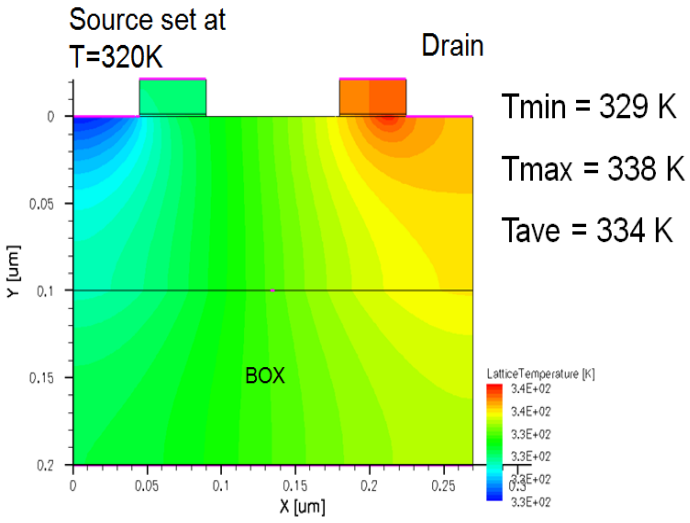
[Sarvari, et al. - IITC'07] [Q. Chen, et al. – IITC'00]

Thermal model





Below device simulation from P. Lim



- Idea: Use V_{DD}/V_{SS} contacts of each gate (in 3D stacked layer) to remove heat from it. Design standard cell library to have low temp. drop within each stacked gate.
- Low (thermal) resistance V_{DD} and V_{SS} distribution networks ensure low temp. drop between heat sink and logic gate
- IntSim+3D: Computes temp. rise of 3D stacked layers using models.

Algorithm used to combine together all these models

1. User inputs parameters
2. Logic gate sizing
3. Select rough initial power estimate
4. Design multilevel interconnect network (including power distribution) for 3D chip with this power estimate
5. Find power predicted by IntSim+3D
6. Is predicted power = initial power? If yes, this is the final interconnect network. If no, choose new initial power estimate = average of previous initial power estimate and IntSim+3D estimate. Go to step 4.
7. Output data

Iterative process used for designing chip

Utility of IntSim+3D

- Pre-silicon optimization and estimation of frequency, power, die size, supply voltage, threshold voltage and multilevel interconnect pitches

- Study scaling trends and estimate benefits of different technology and design modifications

- Undergraduate and graduate courses in universities for intuitive understanding of how a VLSI chip works

IntSim+3D the next generation version of a CAD Tool called IntSim

- IntSim → 2D

  IntSim+3D → Both 2D and 3D

IntSim:

- Developed at Georgia Tech by Deepak C. Sekar, Ragu Venkatesan, Reza Sarvari, Jeff Davis and James Meindl.
- Described in [D. C. Sekar, et al., Proc. ICCAD 2007]
- Used and referenced by multiple researchers at Georgia Tech, UC Davis, Stanford, U. of Illinois at Chicago, Sandia, etc.

Compare 2D and 3D-ICs

22nm node	2D-IC	3D-IC 2 Device Layers	Comments
Frequency	600MHz	600MHz	
Metal Levels	10	10	
Average Wire Length	6um	3.1um	
Av. Gate Size	6 W/L	3 W/L	Since less wire cap. to drive
Die Size (active silicon area)	$50mm^2$	$24mm^2$	3D-IC → **footprint $12mm^2$**
Power	Logic = 0.21W	Logic = 0.1W	Due to smaller Gate Size
	Reps. = 0.17W	Reps. = 0.04W	Due to shorter wires
	Wires = 0.87W	Wires = 0.44W	Due to shorter wires
	Clock = 0.33W	Clock = 0.19W	Due to less wire cap. to drive
	Total = 1.6W	**Total = 0.8W**	

3D with 2 strata → 2x power reduction, ~2x active silicon area reduction vs. 2D