W=Shockley, the Transistor Pioneer—Portrait of an Inventive Genius

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A forensic historian of science and technology suspends Moore's law for a few moments and with the readers embarks on a journey through W=Shockley's (as was his trademark signature) patents to capture a glimpse of his creative mind.

Keywords— *Invention of the transistor, junction transistor, monolithic semiconductor shift register, Moore's law, negative resistance device, semiconductor revolution, Shockley diode, Shockley patents, silicon solar cells, Silicon Valley, switching diode, switching transistor.*

I. INTRODUCTION

In the following 502 pristine handwritten words is described the greatest electrical engineering invention of the twentieth century—a revolutionary invention by W. B. Shockley (Fig. 1) that ushered in the silicon age. The original notebook pages are shown in Fig. 2.

> High Power Large Area Semi-Conductor Valve
>
> The device employs at least three layers having different impurity contents. Suppose there are two layers of N separated by a thin layer of P. Such a device may be produced by evaporation. Ohmic contacts are made to all three layers. Such a structure is indicated diagrammatically on the left.
>
> Under the operating conditions **a** is the emitter; **b**, the control; and **c**, the collector. Modulation by **b** is effected as follows.
>
> In the diagram the potential energy of electrons is shown in the customary way. It is to be observed that there is a potential barrier over which electrons must climb in order to go from **a** to **b**. This barrier is produced by the acceptor impurities in the P-layer. The P-layer is so thin or so slightly excess in P impurities that it does not produce a very high potential barrier. If now a positive potential is applied at **b**, whose contact is such that holes flow easily into the P-layer, these holes will flow into and throughout the P layer thus lowering its potential for electrons. This will increase the flow of electrons over the barrier exponentially. Since the region to the right of the P layer is being operated in the reverse direction, practically all of the electrons crossing the barrier reach it so that the output is essentially high impedance. This will lead to voltage and power gains.
>
> Some current will be drawn by control electrode. However, this will be small compared to the modulated current so long as the concentration of holes in the P-layer is small compared to the concentration of electrons in the high concentration region to the left of the P-layer.
>
> This device can be made into a structure of arbitrary extent in various ways. For example, we can evaporate a layer of N; then a half layer of P; then a grid of metal; the other half layer of P; the second layer of N and the final metal electrode. In

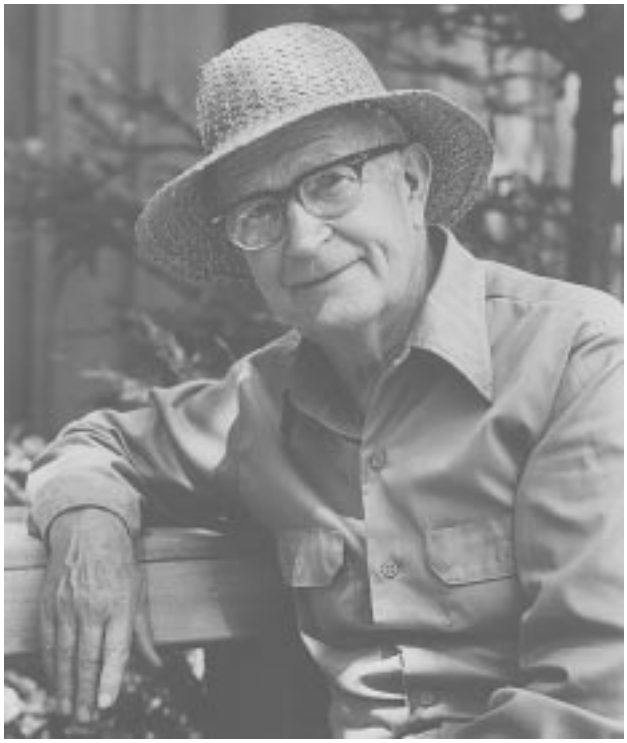

Fig. 1. W. B. Shockley, the scientist who led the semiconductor revolution. (Copyright © Carolyn Caddes.)

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this way a structure such as that shown to the left can be produced. It should be noted that a particularly novel feature is involved in this device. The current path for the carriers of charge lies through material in which the impurities are predominantly of the same sign (i.e., electrons flow thru a region where the impurities are predominantly negatively charged acceptors in the example shown). The net charge in this region is varied by introducing carriers of the opposite sign so as in effect to change the high resistance region in the direction of P-type toward N-type.

In order to obtain ohmic contact it may be desirable to introduce a large concentration of impurities near the metal semiconductor interfaces.

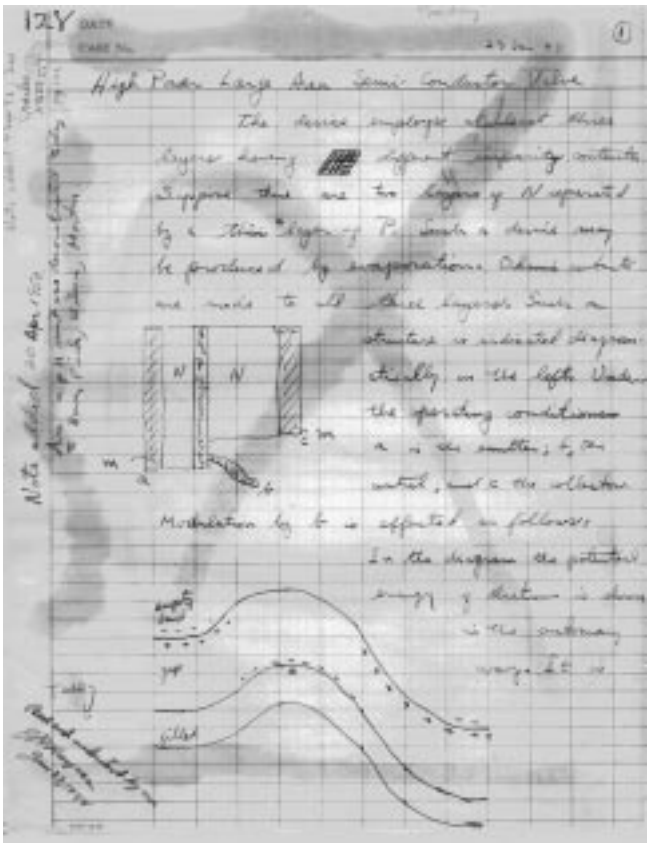
It may also be desirable to concentrate the electron current paths between the grid wires. This may be done by evaporating insulating layers as indicated below. The location of excess impurity layers is also shown.

An approximate expression of Shockley's creativity throughout his professional career as quantified by his yearly patent applications filed and later issued is shown in Fig. 3.

The brilliant revolutionary conception of the junction transistor by Shockley, as shown in Fig. 2, first appeared in a patent application filed on June 26, 1948 (Fig. 4), which was issued in September 1951 (Appendix 1, [12]) and received rigorous mathematical expression in July 1949 (Appendix 2, [34]). In July 1951, the junction transistor became a reality as shown in Fig. 5. Eight years later, in January 1956, the junction transistor, already grown in importance, appeared in the new form of a diffused emitter diffused base silicon junction transistor [2] that could now be fabricated in a batch process, thus being ready for rapid commercialization. The silicon revolution was already on.

A list of 90 patents of Shockley's has been assembled, along with a list of 156 papers and two books, which are presented in Appendixes 1 and 2, respectively. Shockley lived to age 79. Here, we divide his lifetime into six time spans, each of which is briefly described in a section in this paper. In his famous 1976 paper (Appendix 2, [155]), Shockley mentions having some 90-odd patents. This implies that there may be a few more that we do not have listed here. An exhaustive search has not yet been conducted on his patents nor on the list of his published papers in physical sciences.

Shockley's technical contributions are enormous, and a comprehensive discussion of these would require a large amount of time and space that is beyond the scope of this short review. Listing most of his technical publications in one place, however, facilitates detailed study and evaluation by future historians. In this paper, important facts and trends have been skimmed in time sequence to ascertain and evaluate certain major events. For example, from the patent filing structure, one can find how the idea of going into business evolved in Shockley's mind, what the commercial products were that he pursued, and how



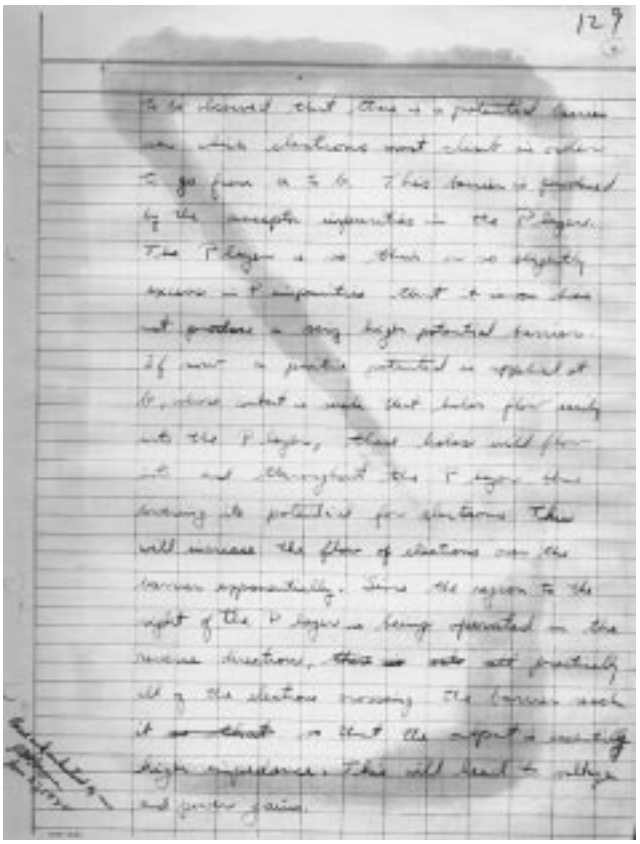
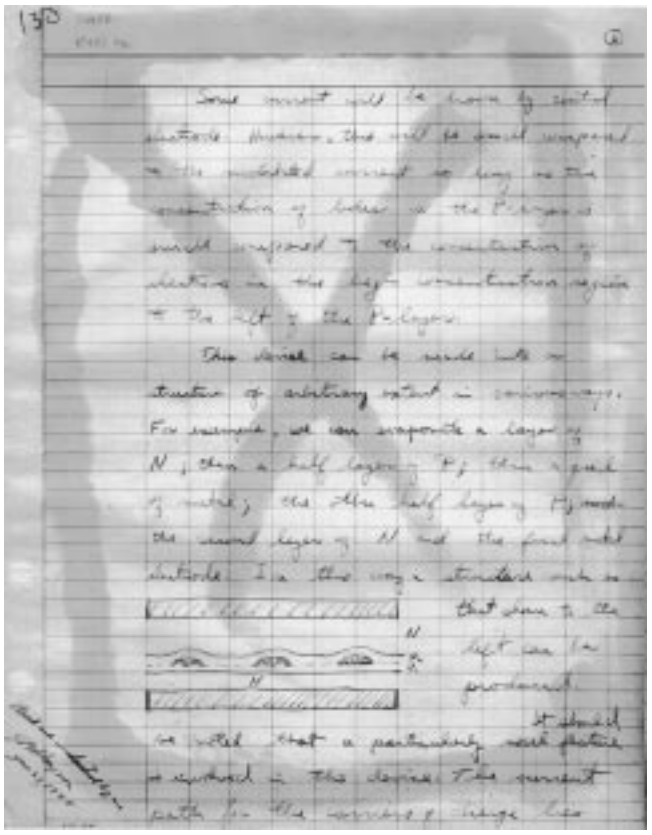


Fig. 2. The greatest electrical engineering invention of the twentieth century. Narrative of the creation of the junction transistor in pp. 128–129 of Shockley's Bell Telephone Laboratories Notebook no. 20 455.



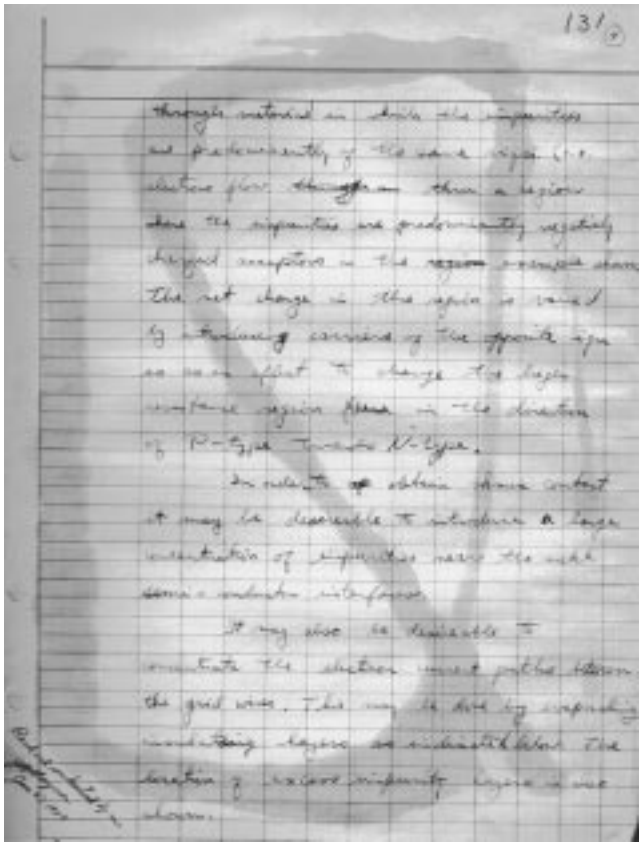


Fig. 2. *(Continued.)* The greatest electrical engineering invention of the twentieth century. Narrative of the creation of the junction transistor in pp. 130–131 of Shockley's Bell Telephone Laboratories Notebook no. 20 455.

Fig. 2. *(Continued.)* The greatest electrical engineering invention of the twentieth century. Narrative of the creation of the junction transistor in p. 132 of Shockley's Bell Telephone Laboratories Notebook no. 20 455.

and why those pursued ideas did not converge toward a sustained successful business venture.

II. The Early Years

Shockley (1910–1989) was the only child of W. H. Shockley (1855–1925) and M. B. Shockley (1879–1977). Shockley was born in London, England, of American parents and lived in Palo Alto, CA, during 1913–1922. He graduated from Hollywood High School, Los Angeles, CA, in 1927 and attended the California Institute of Technology, Pasadena, from which he received the B.S. degree in physics in 1932. Shockley then went to the Massachusetts Institute of Technology (MIT) on a teaching fellowship and received the Ph.D. degree in physics in 1936. His Ph.D. dissertation work was on the "Electronic Bands in Sodium Chloride" and the advisor was Prof. J. C. Slater. Shockley joined Bell Telephone Laboratories (BTL) in September 1936.

III. Shockley at the Bell Telephone Laboratories—The First Period (September 1936–September 1945)

From September 1936 through June 1942, Shockley was involved in research at the Bell Telephone Laboratories

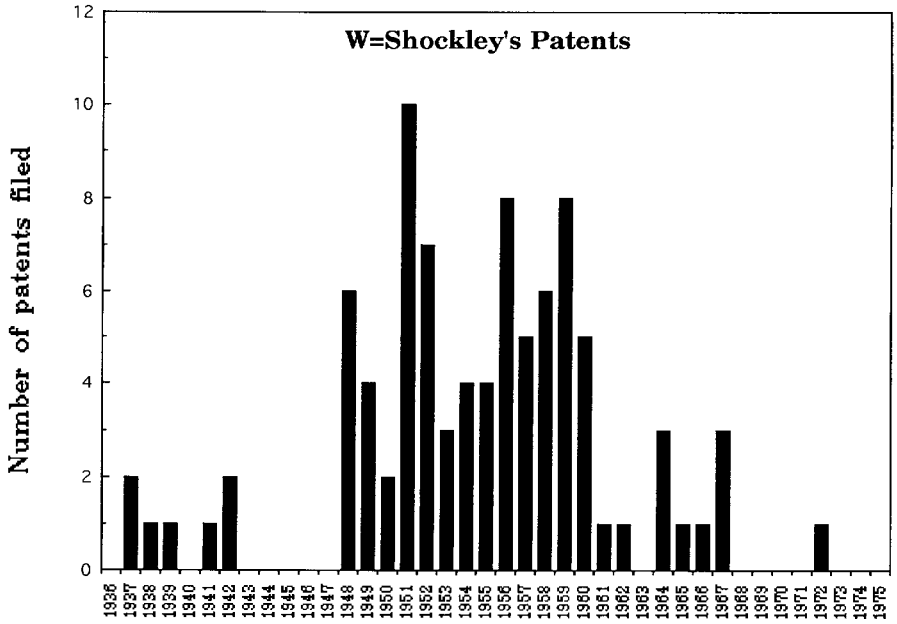


Fig. 3. Creative expression of Shockley's scientific activities as measured in terms of the number of patent applications filed (which were later issued) versus his formal professional years.

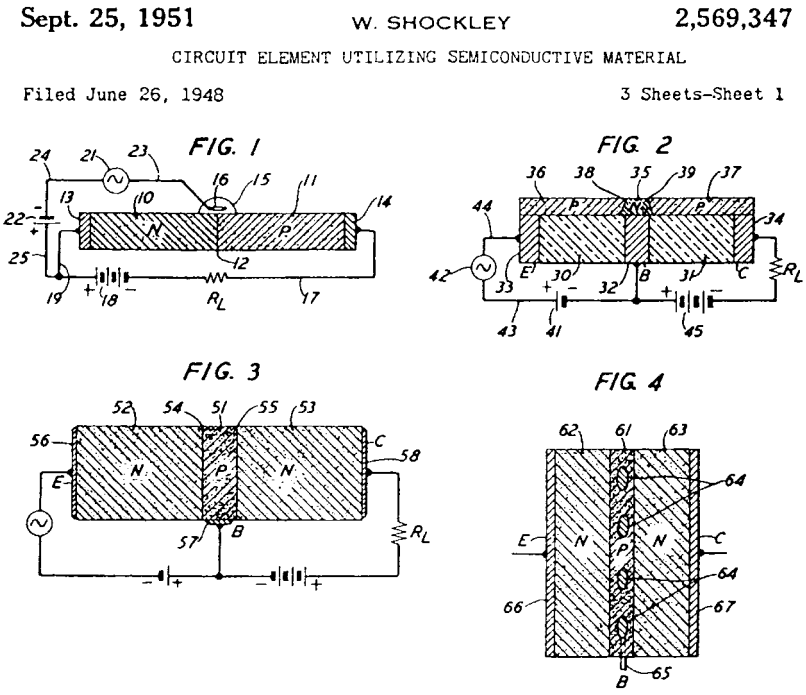


Fig. 4. Schematic of the junction transistor. U.S. Patent 2 569 347.

in Whippany, NJ, and New York, NY. From June 1942 through January 1944 he was director of research, antisubmarine warfare at the Columbia University Division of War Research, Washington, DC. From January 1944 through September 1945, Shockley was an expert consultant at the War Department, Washington, DC.

The following remarks of Shockley's, delivered in his Nobel lecture of December 11, 1956 (Appendix 2, [77]), are of enormous significance in defining the direction of his research and professional activities for the most productive 27 years (September 1936–August 1963) of his life.

> The objective of producing useful devices has strongly influenced the choice of the research projects with which I have been associated. It is frequently said that having a more-or-less specific practical goal in mind will degrade the quality of research. I do not believe that this is necessarily the case and to make my point in this lecture I have chosen my examples of the new

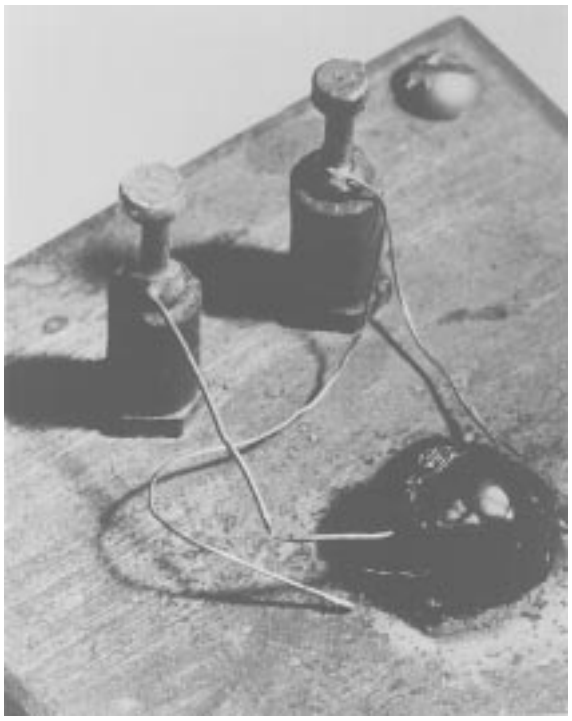


Fig. 5. Picture of the first junction transistor fabricated.

physics of semiconductors from research projects which were very definitely motivated by practical considerations. . . .

My decision to come to Bell Telephone Laboratories immediately after obtaining my Ph.D. in 1936 was strongly influenced by the fact that my supervisor would be C. J. Davisson. Upon my arrival I was assigned by Dr. M. J. Kelly to an indoctrination program in vacuum tubes. In the course of this program Dr. Kelly spoke to me of his ideal of doing all telephone switching electronically instead of with metal contacts. Although I did not choose to continue work on vacuum tubes and was given freedom to pursue basic research problems in solid-state physics, Dr. Kelly's discussion left me continually alert for possible applications of solid-state effects in telephone switching problems. Insofar as my contribution to transistor electronics has hastened the day of a fully electronic telephone exchange, it was strongly stimulated by the experiences given me during my early years at the Laboratories.

These statements defined the guiding force behind Shockley's professional research career in the semiconductor field.

Shockley's technical activities at BTL actually began with work on electron multipliers (Fig. 6) in the Vacuum Tubes Department with J. R. Pierce. Pierce received the Ph.D. degree in electrical engineering from the California Institute of Technology in 1936 and joined BTL at about the same time as Shockley.

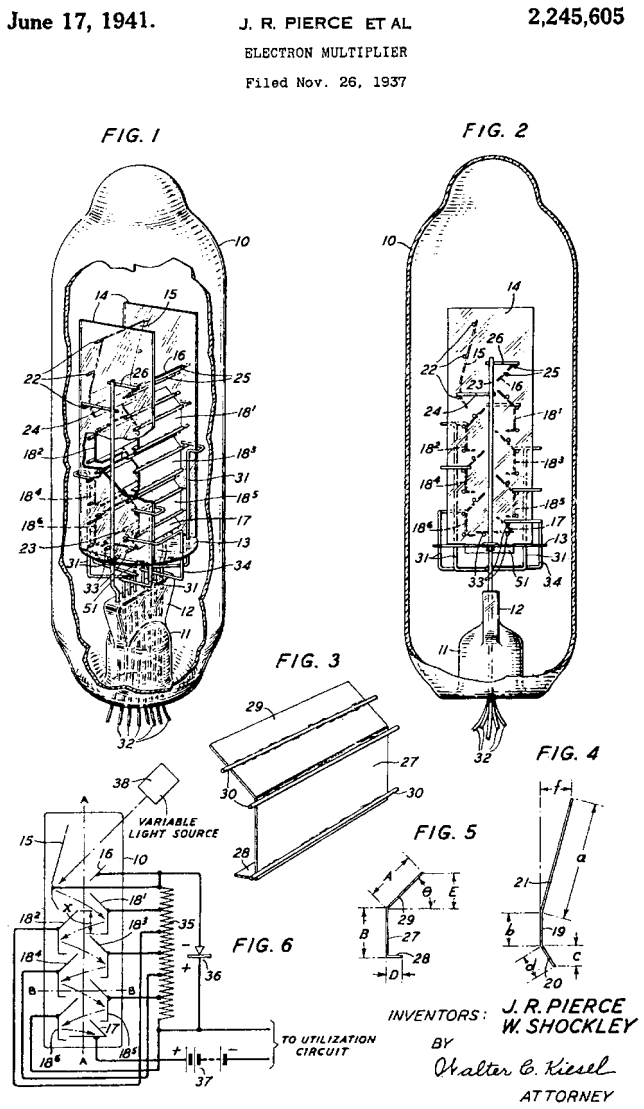


Fig. 6. The electron multiplier tube from the first patent issued jointly to W. Shockley and J. R. Pierce (U.S. Patent 2 245 605).

Shockley had seven patents filed and six issued during this time span. His inventive mind left its mark on the important technical area that he was involved in.

During the Second World War, Shockley invented a precision-guided bombing system and received a patent (Appendix 1, [47]) after the war under the title "Radiant Control System" that employed his previously invented electron multiplier tube (Appendix 1, [1]–[4]). The schematic of Shockley's invention is shown in Fig. 7.

Shockley invented several versions of the electron multiplier tubes (Appendix 1, [1], [2], [4]). His other inventions of this period involved work in ultrahigh-frequency range (Appendix 1, [6]) and precise radio locations of naval vessels like ships and submarines (Appendix 1, [5]).

A. Shockley's Rendezvous with the Bengal Famine (October–December 1944)

During October–December 1944, Shockley spent some time in India as a civilian attached to the U.S. Army–Air

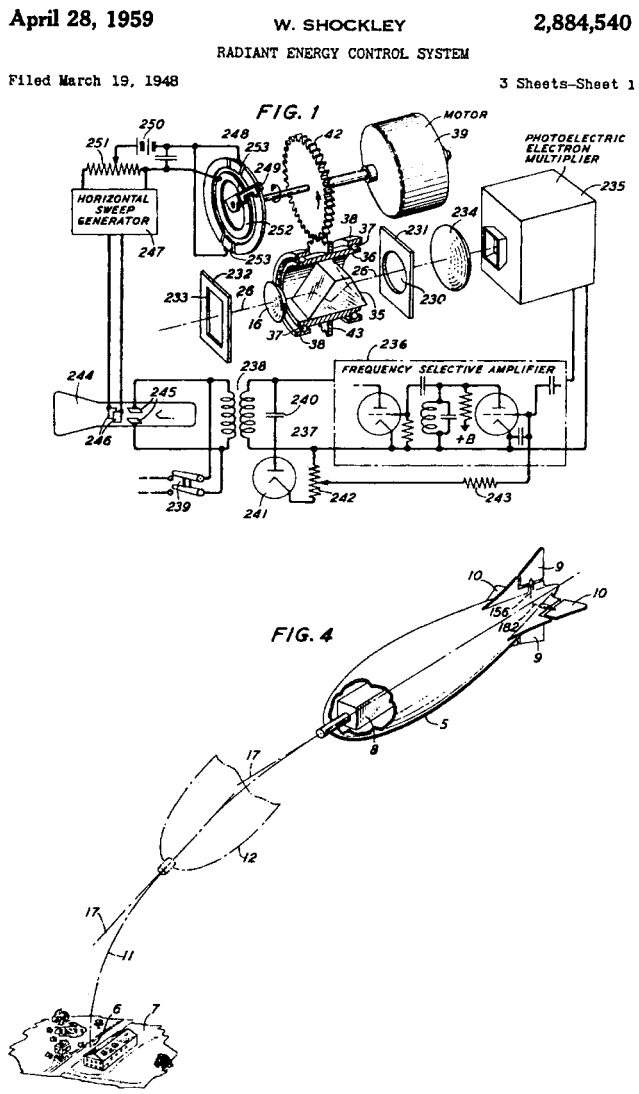


Fig. 7. Shockley's invention of a guided-missile control system that employed the electron multiplier device (U.S. Patent 2 884 540).

Force 20th Bomber Command in Kharagpur, near Calcutta. While there, he witnessed the final stages of the horrors of the Bengal famine of 1943–1944, the artificial famine induced by World War II in which approximately 3 million poor people from the rural areas, coming to the city in search of food, died of starvation in the streets of Calcutta [3]. Scared by the fall of Singapore in 1942 and Burma in 1943, the Allied forces in the Indo-Burma theatre of the Second World War, in preparation for a possible long battle ahead, suddenly withdrew food supply (rice) from the market, purchasing at a higher price and thus creating a severe artificial shortage and causing a sixfold increase in the price of rice at a time when the harvesting was good under normal weather conditions. The poor found their access to food cut off as the prices were beyond reach. Practicing as he preached, defiance in defeat, W. Churchill made no mention of this colossal human tragedy in his *magnum opus* [4], for which he received the Nobel Prize in literature in 1953.

Although it is not clear whether Shockley ever realized the artificial nature of the war-induced famine, he was utterly devastated by this experience in human tragedy. Highly sensitive to humanitarian concerns, Shockley's thoughts and activities during the last third of his life were triggered and shaped by this wartime experience [5].

IV. Shockley at Bell Telephone Laboratories—Semiconductor Device Research (September 1945–August 1955)

From September 1945 to August 1955, Shockley provided the leadership in semiconductor devices research at BTL. This ten-year period was the most productive time in his professional life and one of the most important times in the history of technological revolution. Shockley's publications during this period (Appendix 2, [18]–[74]) show that he was involved simultaneously with several important ideas and projects.

A picture of Shockley with a transistor and a vacuum tube appears in Fig. 8. During this ten-year period, Shockley filed 39 patent applications that were issued, 36 of which were in the transistor area. These patents on transistor devices, processes, and circuits formed the foundation from which the transistor revolution began.

Shockley's transistor-related patents can be loosely classified into five categories. These include:

a) invention of new semiconductor devices;

b) invention of new methods for improving transistor performance in terms of bandwidth, gain (power, voltage, and current), reduced leakage currents, etc.;

c) invention of new fabrication processes or improvements thereof;

d) invention of new semiconductor circuit applications;

e) invention of modified techniques of crystal growth for fabricating better semiconductor devices with graded impurity crystals.

These patents are very briefly described below.

A. The Semiconductor Device Patents

Shockley is known worldwide as the inventor of the bipolar junction transistor and the unipolar junction transistor or junction field-effect transistor. Shockley also invented semiconductor negative resistance devices, switching transistors, and semiconductor infrared energy sources, which are outlined next.

1) The Original Junction Transistor Patents: Shockley's first application for a patent in the semiconductor field is his most famous junction transistor patent (Appendix 1, [12]) based on his revolutionary invention of the minority carrier injection concept in bipolar transistor action on January 23, 1948. The application for the first junction transistor patent was filed on June 26, 1948. This original patent application was divided and continued in part to produce two additional patents (Appendix 1, [14], [21]). The second patent (Appendix 1, [14]) (filed May 5, 1949), contained additional

Fig. 8. Shockley with a transistor and vacuum tube.

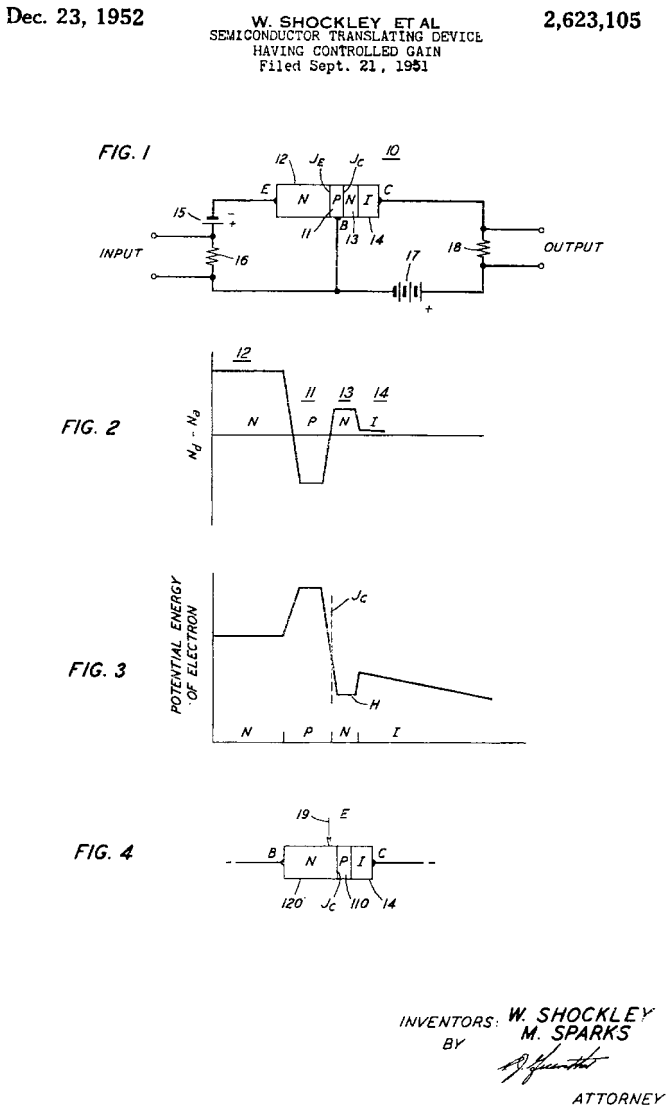


Fig. 9. Shockley and M. Sparks' invention of the junction transistor with a hook collector to provide intrinsic current multiplication factor of greater than unity (U.S. Patent 2 623 105).

claims, including an additional layer in the collector region, whereas the third patent (Appendix 1, [21]) (filed May 28, 1949), included additional claims on semiconductor oscillator circuits based on the junction transistor.

Before the first junction transistor patent was issued, two of Shockley's other semiconductor amplifier patents (Appendix 1, [8], [9])—both of whose applications were filed on September 24, 1948, after some important experiments (including the famous Shockley–Haynes experiment) were conducted and one of which was coauthored by G. L. Pearson—were issued on April 4, 1950, some six months before the original point-contact transistor patent of J. Bardeen and W. Brattain was issued [6].

Shockley's first issued single-author transistor patent (Appendix 1, [9]) is a hybrid transistor consisting of a collector-base p-n junction with a point-contact emitter. In another patent (Appendix 1, [13]), filed also on September 24, 1948, Haynes and Shockley described the invention of the early hybrid transistor with controlled carrier transit times.

Fig. 9 depicts an important invention of a transistor (Appendix 1, [15]) with a "hook collector" that could provide an intrinsic current multiplication factor of greater than unity. This invention was created with M. Sparks and is described in U.S. Patent 2 623 105 (filed September 21, 1951). It is directly related to Shockley's later invention of the four-layer p-n-p-n switching diode.

2) The Unipolar Junction Transistor (UJT) Patents: With the motivation to improve the high-frequency characteristics of junction transistors, Shockley invented the unipolar junction transistor or junction field-effect transistor (Appendix 1, [27]), where the majority carrier is the dominant current carrier that decreases the carrier transit delay. The original UJT patent (U.S. Patent 2 744 970) was filed on August 24, 1951. Further improvements on the performance of the UJT are contained in two additional patents (Appendix 1, [31], [35]). In U.S. Patent 2 764 642 (filed October 31, 1952), UJT characteristics are made uniform and more reproducible by constructing the space between the source and drain zones as smaller and accurately controllable. In U.S. Patent 2 778 885 (also filed October 31, 1952), UJT input–output relations are made more controllable and stable by constructing the portion of the N-type semiconductor body adjacent to the drain more strongly N-type to suppress the flow of minority carriers from there.

3) Semiconductor Negative Resistance Device Patents: One important subject that fascinated Shockley throughout his transistor career was the negative resistance phenomenon in semiconductor devices arising out of carrier transit

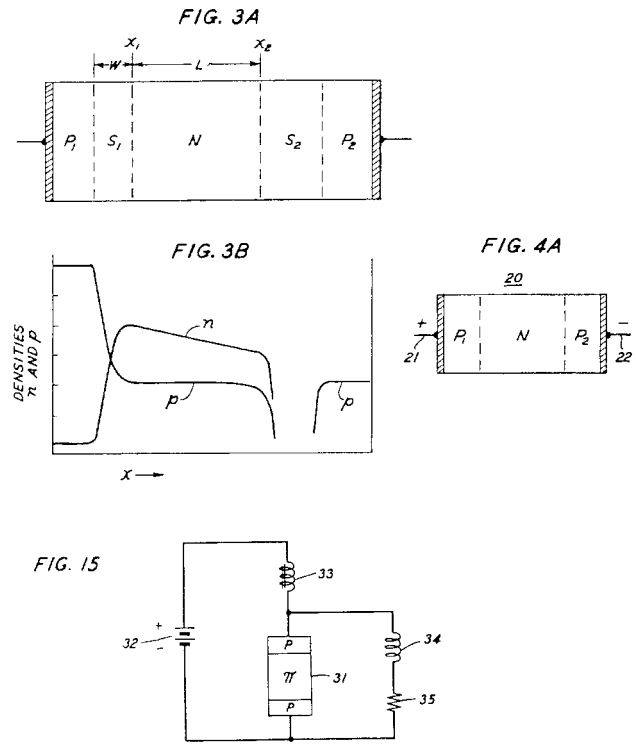


Fig. 10. Shockley's invention of the negative resistance semiconductor device arising out of transit time delay (U.S. Patent 2 772 360).

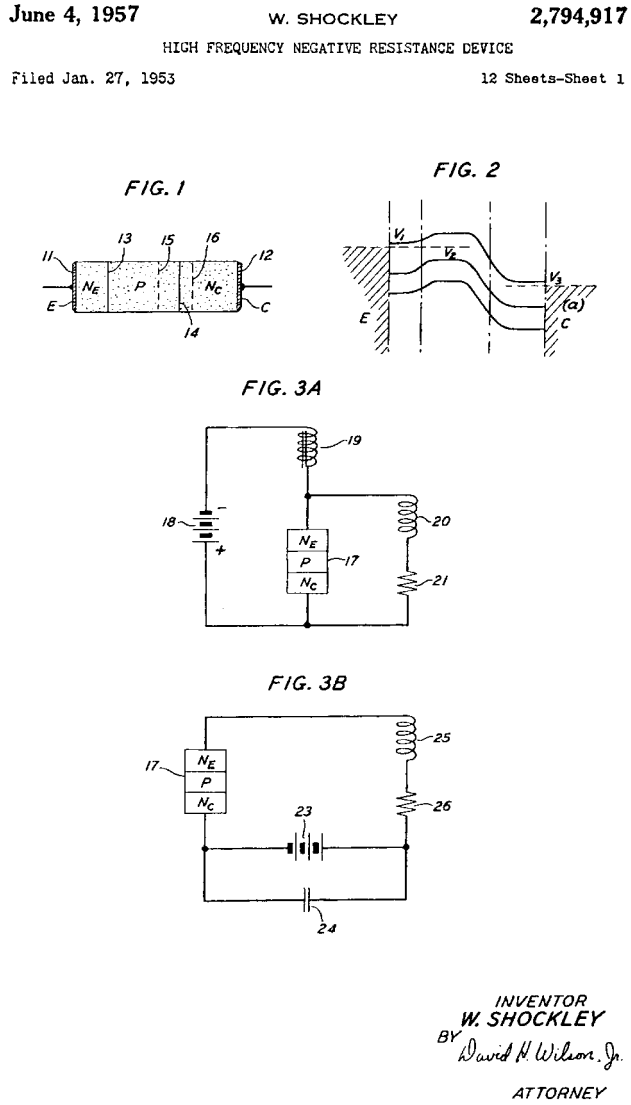


Fig. 11. Shockley's invention of the high-frequency negative resistance semiconductor device arising out of transit time delay (U.S. Patent 2 794 917).

time delay. His invention of the negative resistance device and its applications are described in U.S. Patents 2 775 658 (Appendix 1, [33]) and 2 794 864 (Appendix 1, [38]). The invention of the high-frequency version of the negative resistance device is described in U.S. Patent 2 794 917 (filed January 27, 1953) (Fig. 11). Further applications and refinements are described in U.S. Patent 2 772 360 (filed February 11, 1954) (Fig. 10) and, on its high-frequency version, in U.S. Patent 2 852 677 (filed June 28, 1955)—the last patent filed from this ten-year BTL period of Shockley's semiconductor device research.

4) The Infrared Energy Source Patent: In U.S. Patent 2 683 794 (filed December 27, 1951), Shockley, along with coinventors Briggs and Haynes, described the invention of a new infrared energy source based on hole-electron recombination in germanium and silicon p-n junctions. Housed in a cryogenic Dewar flask to remove thermal effects, the infrared source had specific narrow spectral lines related to the band-gap energies in the specific semiconductors.

Work along these lines during the next ten years with compound semiconductors led to the invention of p-n junction light-emitting diodes and solid-state laser diodes.

B. The Device Performance Improvement Patents

Four of Shockley's transistor patents (Appendix 1, [20], [28], [37], [40]) were devoted to improving the performance characteristics of the junction transistor. In U.S. Patent 2 672 528 (filed May 28, 1949), reduction in leakage currents was suggested with improved fabrication techniques and geometries. U.S. Patent 2 756 285 (filed August 24, 1951), used a semiconductive body of filamentary forms to make the transistor device suitable for amplification at high frequencies on the order of 10 MHz. U.S. Patent 2 790 037 (filed March 14, 1952), dealt with improvements in current gain as well as high-frequency response. In U.S. Patent 2 813 233 (filed July 1, 1954), improved frequency response was achieved with reduced base resistance.

C. The Process Patents

Shockley made original contributions toward the conception and realization of junction transistors employing the diffusion process and ion-implantation process, the two most important processes of fabricating discrete transistors and monolithic integrated circuits.

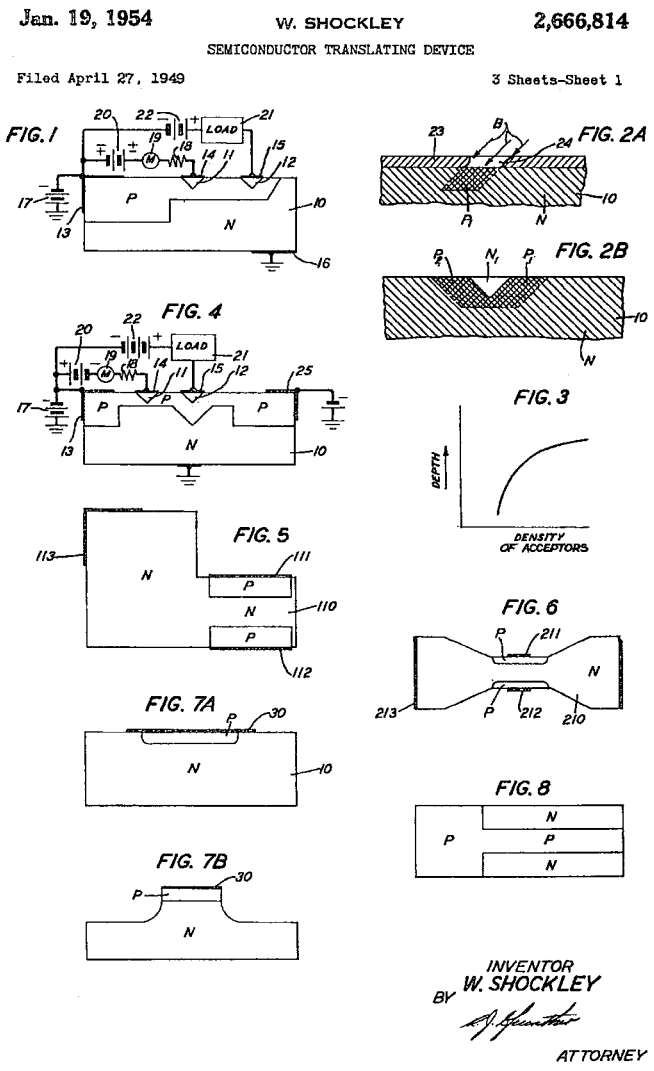


Fig. 12. Shockley's inventive idea of forming p-n junctions with nuclear bombardment (U.S. Patent 2 666 814).

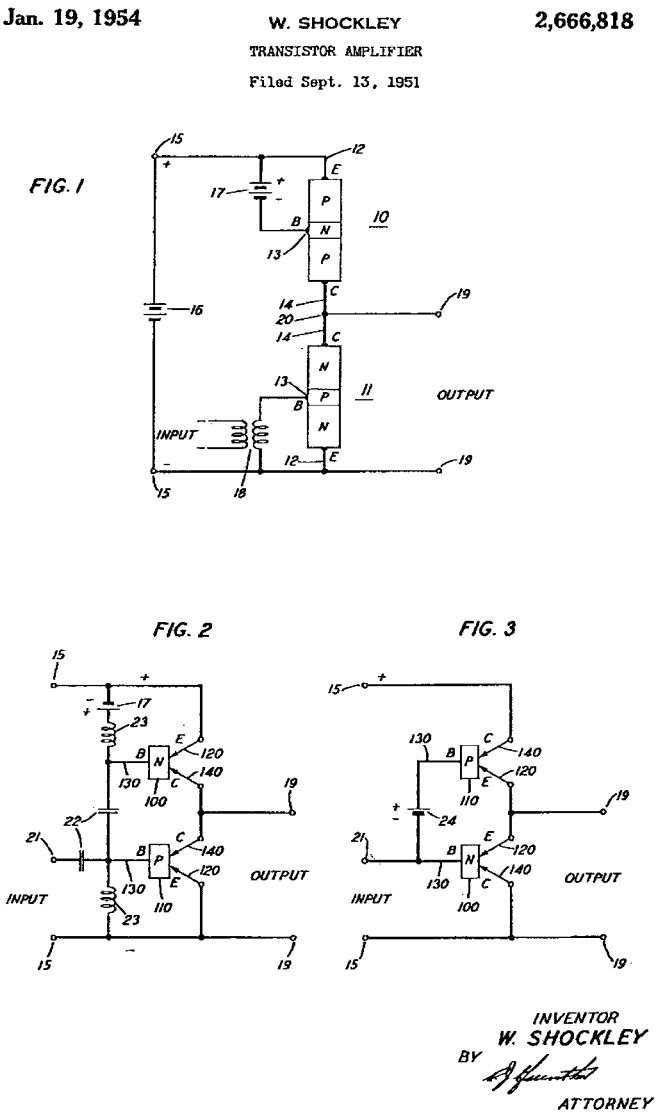


Fig. 13. Shockley's invention of the p-n-p/n-p-n complementary symmetry pair as a push-pull amplifier (U.S. Patent 2 666 818).

1) Diffusion Process: The application of the diffusion process in creating junction transistors was first described in Shockley's original patent (Appendix 1, [12]) application of June 26, 1948.

Shockley's inventive contributions toward practical realization of transistors using the diffusion process are primarily contained in three patents (Appendix 1, [41], [44], [65]). In U.S. Patent 2 816 847 (filed November 18, 1953), Shockley proposed coating the semiconductor crystal with a thin layer of the impurity material and then fabricating a thin layer of the desired type (n or p) by heating the surface with an electron beam, causing diffusion of the impurity material in designated areas by the correct amount. In U.S. Patent 2 868 678 (filed March 23, 1955), Shockley proposed the method of forming large-area p-n junctions using a diffusant impurity element in a suitable carrier to improve the high-frequency performance of the resulting transistors. In U.S. Patent 3 028 655 (filed March 23, 1955), Shockley proposed providing a proper concentration gradient of impurity atoms in the base region for high-frequency operations.

2) Ion-Implantation Process: Shockley is known as the inventor of the ion-implantation process for fabricating junction transistors (Appendix 1, [36]). Long before this patent application (U.S. Patent 2 787 564) was filed on October 28, 1954, Shockley first proposed the fabrication of junction transistors using nuclear bombardment (Fig. 12) of deuteron and alpha particles (Appendix 1, [18]). That patent application (U.S. Patent 2 666 814) was filed on April 27, 1949, about a year before the first functioning alloy junction transistor came into existence.

D. The Circuit Application Patents

During this time period, Shockley had filed for and obtained 11 patents that belonged to the circuit applications category. The first patent (Appendix 1, [11]) (filed April 27, 1950), is on a new acoustic transducer based on the Suhl effect that deals with the effect of magnetic field on the charge carrier flow through a semiconductor bar with possible applications in microphones. Shockley is

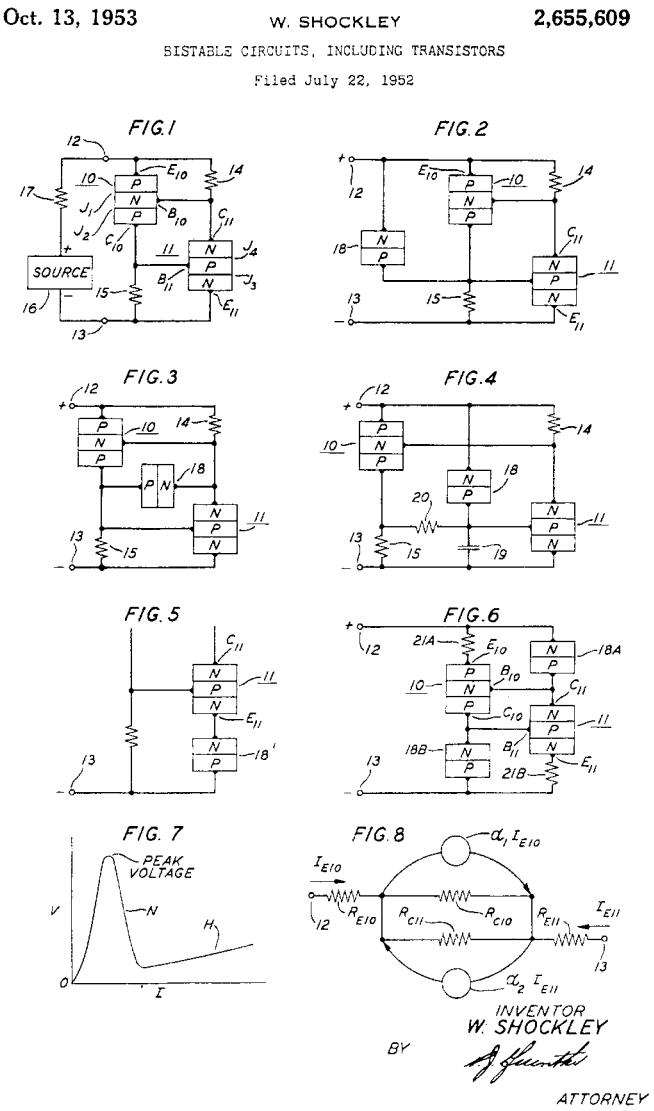


Fig. 14. Shockley's invention of the p-n-p/n-p-n complementary symmetry pair as a bistable transistor switch (U.S. Patent 2 655 609).

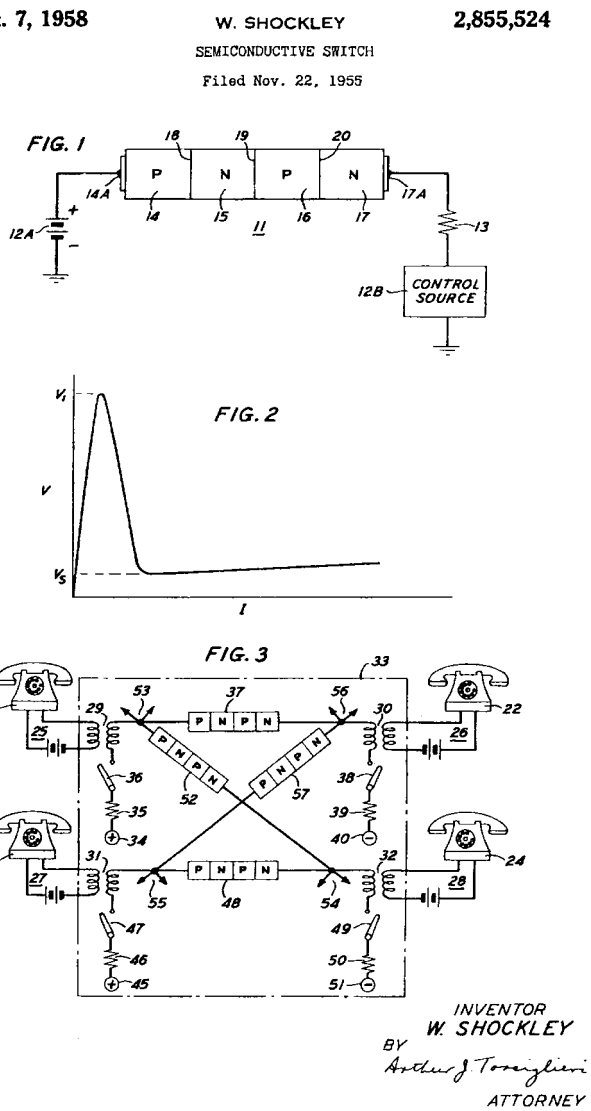


Fig. 15. Shockley's invention of the P-N-P-N four-layer switching diode and its application as a telephone-line cross-point switch (U.S. Patent 2 855 524).

the inventor (Appendix 1, [19]) of the complementary symmetry n-p-n/p-n-p transistor pair amplifier (Fig. 13) (U.S. Patent 2 666 818, filed September 13, 1951). Shockley also invented the binary flip-flop (Fig. 14) based on the nonlinear (digital) region operation of the complementary symmetry pair of n-p-n/p-n-p transistors (Appendix 1, [17]) (U.S. Patent 2 655 609, filed July 22, 1952). These two original inventions have no prior counterparts in vacuum tubes.

In U.S. Patent 2 714 702 (Appendix 1, [24]) (filed February 16, 1951), Shockley proposed pulse-shaping circuits based on reverse p-n junction breakdown of transistors. U.S. Patent 2 716 729 describes transistors based on constant current source (Appendix 1, [25]) (filed November 24, 1951). Shockley invented frequency-selective semiconductor circuits (Appendix 1, [29]) based on conductivity modulation generated by semiconductors with modulated surfaces (U.S. Patent 2 761 020, filed September 12, 1951). The invention of a transistorized class-B amplifier (Appendix 1, [30]) by Shockley is described in U.S. Patent 2 763 832 (filed July 28, 1951).

The basic phenomenon of negative resistance arising in carrier transports in semiconductors was utilized by Shockley to invent (Appendix 1, [34]) the asymmetric waveguide structure in U.S. Patent 2 777 906 (filed June 26, 1953), and the Hall-effect-based nonreciprocal transducer (Appendix 1, [38]) in U.S. Patent 2 794 864 (filed August 1, 1952). Shockley also invented a new and improved transistor switching circuit (Appendix 1, [49]), described in U.S. Patent 2 891 171 (filed September 3, 1954), that removed spurious signals generated during the switching transition.

E. The Modified Crystal Growing Patent

In U.S. Patent 2 730 470 (filed June 15, 1950), Shockley proposed (Appendix 1, [26]) a method of producing single crystals of germanium successive zones of N and P conductivity types, respectively, wherein the conductivity of each

zone is graded with respect to the p-n junction between the two zones.

In addition to the above-mentioned patents, Shockley's other inventions include U.S. Patent 2 654 059 for making good base connections (Appendix 1, [16]) in a junction transistor (filed May 26, 1951).

In U.S. Patent 2 696 565 (filed November 6, 1952), an electrooptical control system is described (Appendix 1, [23]) by Shockley for automatic positioning of two or more objects by means of electrical control signals generated by comparison of two optical patterns. During the Second World War, Shockley invented a differential altimeter (U.S. Patent 2 509 889, filed January 13, 1948) for measuring the accurate height of airplanes (Appendix 1, [10]). Changing air pressure causes an air flow through a very narrow tube opening into a large closed vessel. A heating element placed between two thermistor elements in the narrow tube will cause a signed differential voltage generated between the two thermistor elements caused by the directed air flow. This can be measured to indicate descending or ascending altitude.

From February 1954 to July 1954, Shockley was a visiting professor of physics at the California Institute of Technology, Pasadena. From July 1954 to August 1955, he was back at BTL in charge of transistor physics research. It is during this time period that his ideas of embarking on a business venture developed.

Two specific things in semiconductor devices had fascinated Shockley throughout his active career in the transistor field. One is the n-p-n/p-n-p transistor combination, on which he invented a bistable circuit, and the other was the negative resistance phenomenon in semiconductor devices arising out of carrier transit time delay. Theoretical and experimental works on these two subjects led to the invention of the Shockley diode, the p-n-p-n four-layer device whose enormous commercial potential perceived at that time led Shockley to venture into business activities in California.

V. Shockley's California Business Venture (September 1955–August 1963)

Shockley's decision to leave BTL to get personally involved in the commercialization of his transistor inventions is an epoch-making event in the history of the technological revolution in the second half of the twentieth century, as it directly led to the emergence of the silicon transistor industries in the San Francisco Bay area now popularly known as Silicon Valley. An authentic presentation and analysis of the sequence of events is of immense historical interest.

In 1955, Shockley left BTL to join Beckman Instruments, Inc., and to establish Shockley Semiconductor Laboratory in Palo Alto, CA, for research, development, and production of new transistor and other semiconductor devices. This became the Shockley Transistor Corporation, a subsidiary of Beckman Instruments, in 1958. In April 1960, this organization was acquired by the Clevite Corporation, and Shockley became the director of Shockley Laboratories, a unit of Clevite Transistor of the Clevite Corporation of Ohio. After being appointed to the chair professorship at Stanford University, CA, Shockley continued as a consultant to the Shockley Laboratories of Clevite Transistor until its sale to International Telephone and Telegraph (ITT) in 1965.

Shockley's primary goal was to manufacture the four-layer Shockley diodes as electronic switches with applications in telephone communications. The following communication with a Stanford University professor on February 28, 1956, makes that particularly clear. Shockley wrote to the professor:

> I would like you to try to invent new circuit applications for a device which we are considering manufacturing. This device is a two-terminal semiconductor device similar in operating characteristics to the NPN plus PNP transistor combination which I have previously invented. This device can act as a cross point and perform circuit functions similar to gas discharge tubes. However, its superior ratio of breakdown to sustain voltage will enable it to operate in some cases where gas discharge tubes cannot. For this reason, it seems probable that previously insolvable switching problems will now be solvable. We are eager to obtain a good patent position with respect to applications of this device and I should like to obtain your consulting services to whatever degree you and I agree to be appropriate in periodic discussions.
>
> Such inventions as you do make will be the property of the Shockley Semiconductor Laboratory, and we shall expect you to assist us in obtaining patents on such applications at our expense.
>
> Since the decision to pursue such a device actively is an important one for our company, you will of course understand that we do not wish knowledge of our interest in this device to go to individuals who have not signed a patent agreement with us.

Toward this end, he applied for a patent describing its application as a telephone-line cross-point switch. This was the first patent that he applied for soon after coming to California in September 1955. This important patent is shown in Fig. 15. Shockley within the first year assembled a group of first-class scientists. Two pictures depicting this group of scientists and other support personnel are shown in Figs. 16 and 17. They had assembled to celebrate Shockley's winning the Nobel Prize in physics in 1956, which he shared with Bardeen and Brattain. Fig. 18 shows Shockley along with his mother and wife en route to Stockholm to receive the Nobel Prize. Fig. 19 shows the award ceremony.

A picture of the real Shockley diode is shown in Fig. 20. Shockley invented another use of the diode in the form of a novel shift register (Appendix 1, [50], [56]), which is shown in Fig. 21.

The shift register patent (Appendix 1, [56]) carries the idea of a monolithic digital circuit and is the first patent

Fig. 16. The transistor guru and his disciples celebrating Shockley's winning the Nobel Prize in physics in 1956. First on the left sitting is G. E. Moore, currently Chairman Emeritus of Intel Corporation. Standing fourth from the right is R. N. Noyce and standing at the extreme right is J. T. Last.

Fig. 17. Celebrating Shockley's winning the Nobel Prize in physics, 1956, are some of the employees of Shockley Semiconductor Laboratory. With Shockley in the picture at the extreme left is C.-T. Sah. On the extreme right sitting is J. A. Hoerni.

describing the dawn of the monolithic idea in the evolution process of monolithic integrated circuits [10], [11]. The historic timeline of the evolution of the monolithic integrated circuit is shown in Fig. 22. The patent itself is shown in Fig. 31.

Shockley began manufacturing and selling Shockley diodes in 1958–1959. In applications involving solid-state circuits, however, this two-terminal device came in direct competition with Shockley's very own junction transistors manufactured by several companies within the United States. Shockley as the inventor remained enchanted by the elegance and commercial potential of this two-terminal device, but its large-scale manufacture with reproducible characteristics continued to be difficult. The following letter, a copy of which was sent to Shockley, poignantly describes why the Shockley diode was not commercially successful.

Fig. 18. En route to Stockholm to receive the Nobel Prize, December 9, 1956. On the left is Shockley's second wife, E. L. Shockley. In the middle is Shockley's mother, M. B. Shockley.

Date: September 21, 1960

To Frank Newman
Shockley Transistor Corporation

Dear Frank:

I talked with Bill Gunning today concerning the use of our diodes in their North American Aviation Job. They have made the decision to abandon Shockley diodes in this project. In going through their circuitry, they found that 100 of the Shockley units failed with the temperature increased to their top limit. I believe these failures were failure to turn off. Also, they found that the holding current drifted for 100 units to a point where it was intolerable. 50 of the above 200 units were overlapping so that a total of 150 units were unusable.

At this point, they decided that rather than replace these units, they would redesign the entire system. This, of course, is very unfortunate from our standpoint as well as theirs. It requires the redesign of all the boards, as well as new boards.

To make the cheese more binding, they find that by using transistors at today's fallen prices, they can do it less expensively than they could with Shockley diodes. They are buying a G.E. transistor for $0.90 each.

Best regards,
(Len Winters)

Fig. 19. Shockley receiving the Nobel Prize in physics, December 10, 1956. Observing on the right is Bardeen.

During this eight-year period, Shockley remained a prolific inventor and filed applications for 35 patents, which were duly granted (Appendix 1, [43], [45], [46], [48], [50]–[64], [66]–[80], [82]). The contents of all of these inventions are not discussed here. Some are described, however, in Figs. 24–28. As seen in Fig. 27, Shockley's attention during this eight-year period was focused also on p-n-junction-based high-efficiency solar-cell design that found ready applications in satellite systems as well as in pocket calculators developed in later years.

Two years into its operation, a group of eight scientists from Shockley Semiconductor Laboratory left to start a new company to manufacture and sell Shockley's greatest invention: the junction transistor. It came into existence as Fairchild Semiconductor in the middle of September 1957. The mastermind of this effort was G. E. Moore [7], [8]. This development of the creative fission process is one of the most important technological events of the twentieth century and the first one in a periodic series that created Silicon Valley [9].

Immediately after arriving in California, Shockley began assembling the scientists to carry out the transistor research and development work. The most important scientist for the chemically based electronic device that is the transistor is the physical chemist. Shockley wanted M. Sparks, who brought into existence the first junction transistor, to come to California and join him. But Sparks was happy with BTL and did not leave. Shockley also wanted M. Tanenbaum to join him in California. Tanenbaum had just brought into

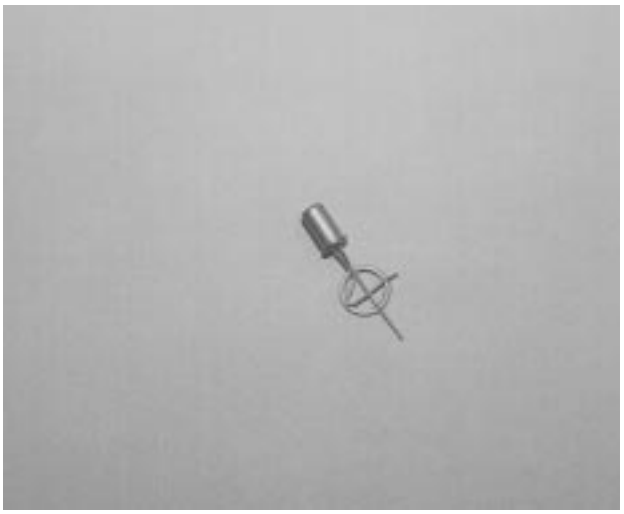


Fig. 20. A picture of the Shockley diode.

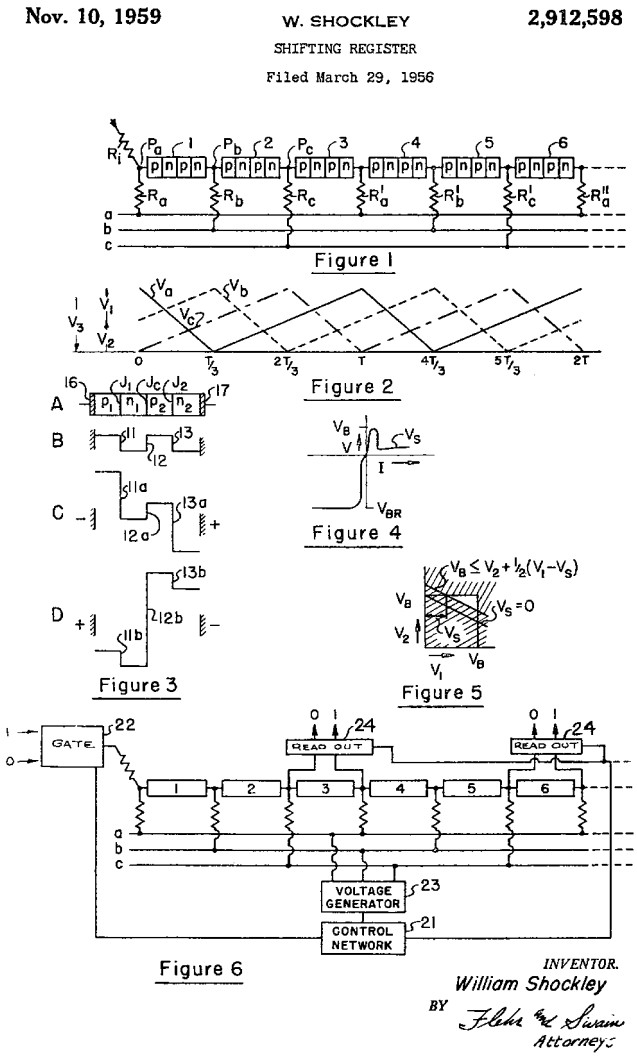


Fig. 21. Shockley's invention of the semiconductor shift register with four-layer p-n-p-n diodes (U.S. Patent 2 912 598).

existence the diffused emitter and base silicon transistors [2] that provided a major technological breakthrough toward realization of batch-fabricated silicon junction transistors. In October 1955, Shockley engaged his friend J. Rabinow

Historic time line on the evolution of the monolithic integrated circuits.

Date	Event
April 25, 1956	William B. Shockley files for patent on *Semiconductor Shift Register*
September 1957	Robert N. Noyce joins Fairchild Semiconductors
May 1958	Jack S. Kilby joins *Texas Instruments*
February 6, 1959	Jack S. Kilby files for patent on *Miniaturized Electronic Circuits*
July 30, 1959	Robert N. Noyce files for patent on *Semiconductor Device-and-Lead Structure*
January 10, 1961	William B. Shockley obtains patent on *Semiconductor Shift Register U.S. Patent No. 2,967,952*
April 25, 1961	Robert N. Noyce obtains patent on *Semiconductor Device-and-Lead Structure. U.S. Patent No. 2,981, 877*
June 23, 1964	Jack S. Kilby obtains patent on *Miniaturized Electronic Circuits U.S. Patent No. 3,138,743*

Fig. 22. Historic timeline of the evolution of the monolithic integrated circuit.

in Washington, DC, to help in getting Tanenbaum to go west. Nevertheless, Tanenbaum too was very happy with his position at BTL and did not leave. Shockley finally discovered a brilliant young physical chemist, a California Institute of Technology Ph.D. (and currently chairman of the Board of Trustees there) in Moore [Fig. 23(a)].

When Moore joined the Shockley Semiconductor laboratory, he had no prior involvement with transistors. Moore was in knowledge-acquisition mode when he discovered shortly that in a research project that Shockley had initiated in a corner of his laboratory, Shockley had divided his small research group into two subgroups, of which only one was authorized to know what was going on there and the other was not. This situation made Moore very unhappy, as he was being placed in the latter group. This event acted as the catalyst in the process that eventually led to his departure from Shockley Semiconductor [12] in September 1957 along with seven others, including Noyce [Fig. 23(b)], the physicist who provided the technical leadership with his greater knowledge of the transistor manufacturing process.

VI. Stanford University Years (September 1963–February 1975)

In August 1963, Shockley was appointed to the Alexander Poniatoff Chair as professor of engineering science at Stanford University. As mentioned, he remained a consultant to the Shockley Transistor unit of the Clevite Corporation for the next two years until 1965, when the unit was sold to ITT.

(a)

(b)

Fig. 23. (a) G. E. Moore. (b) R. N. Noyce. These two men, along with six other employees of Shockley's, went on to found Fairchild Semiconductor to commercialize Shockley's creature, the junction transistor, on a war footing, leading to the creation of what is now known as Silicon Valley in California. (Copyright © Carolyn Caddes.)

The research works in the semiconductor field and other areas are described in Appendix 2, [130]–[154]. From the work done during the two-year period September 1963–August 1965, Shockley filed and obtained four patents (Ap-

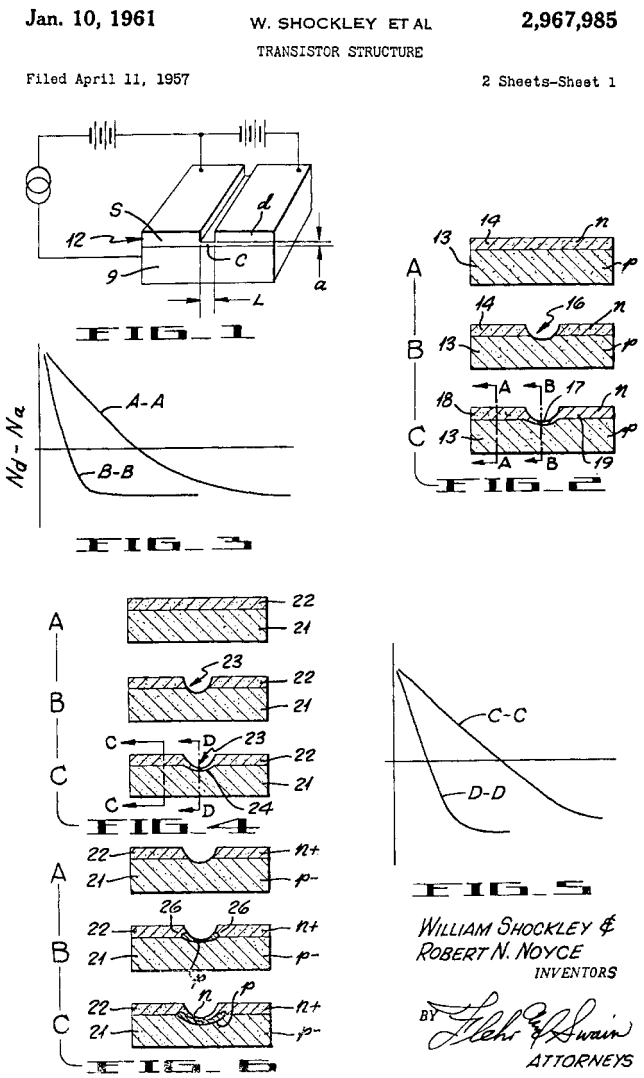


Fig. 24. Shockley and Noyce's joint patent on an improved junction field-effect transistor (U.S. Patent 2 967 985).

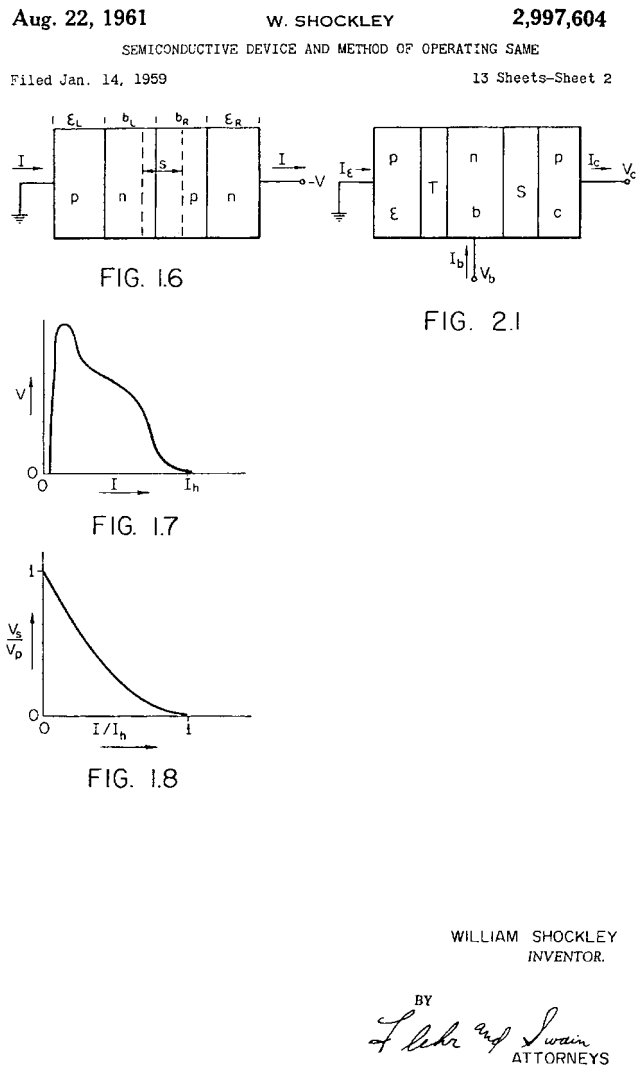


Fig. 25. Shockley's master patent containing the theory and applications of the p-n-p-n four-layer semiconductor switching diode device (U.S. Patent 2 997 604).

pendix 1, [81], [83], [84], [86]). One of these (Appendix 1, [81]) discusses methods of improving the performance of four-layer p-n-p-n diodes by making them immune to degrading surface conditions affecting the breakdown voltage and leakage currents (Fig. 28). Shockley indeed did his level best to the end to make the Shockley diodes work reliably. The second patent (Appendix 1, [83]) describes the invention of a surface-controlled avalanche transistor for high-frequency, high-power operation in which the control terminal draws no current. Another invention is a noise diode (Appendix 1, [84]), which provides a stable noise output from an avalanche diode and is insensitive to temperature variations. The fourth invention (Appendix 1, [86]) is a transistor for high-frequency operation wherein, as the title indicates, current is carried by the same type of carrier in all said regions.

A. Shockley at Bell Telephone Laboratories: The Later Years (1965–1975)

The patent in Appendix 1, [85] is a stable improved piezoelectric resonator. The patent in Appendix 1, [90] is for transistor-operated chopper devices and circuits, taken out with one of his students.

In 1965, Shockley renewed his association with BTL as an executive consultant. In that capacity, he became involved with research and development work for thin-film magnetic bubble memory systems. He was a coinventor of three patents issued on the subject (Appendix 1, [87]–[89]). The patent that involved the design of a thin-film magnetic bubble shift register for applications in the computer field is shown in Fig. 29.

VII. Shockley's Later Years (March 1975–August 13, 1989)

Shockley formally retired from his academic position with Stanford University as well as his executive consultant's position with BTL in 1975 upon reaching the age of 65 and thereafter was Emeritus Professor at Stanford until his death in August 1989. During these remaining 14 years of his life, Shockley's major lasting contribution in the transistor field was the historical paper "The Path

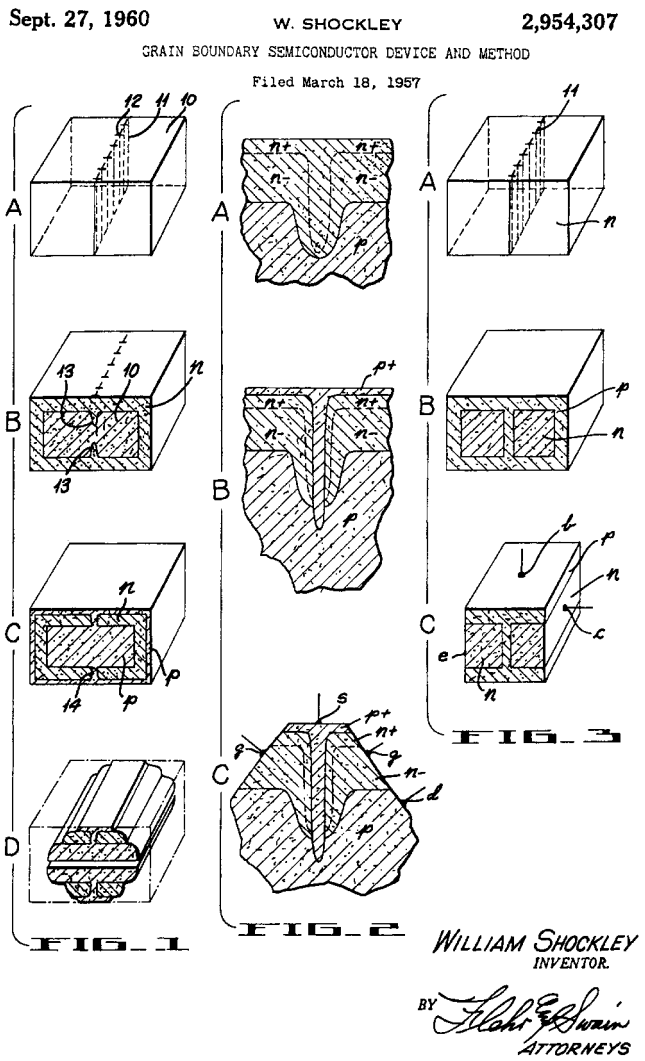


Fig. 26. Shockley's invention of the grain boundary semiconductor device and method (U.S. Patent 2 954 307).

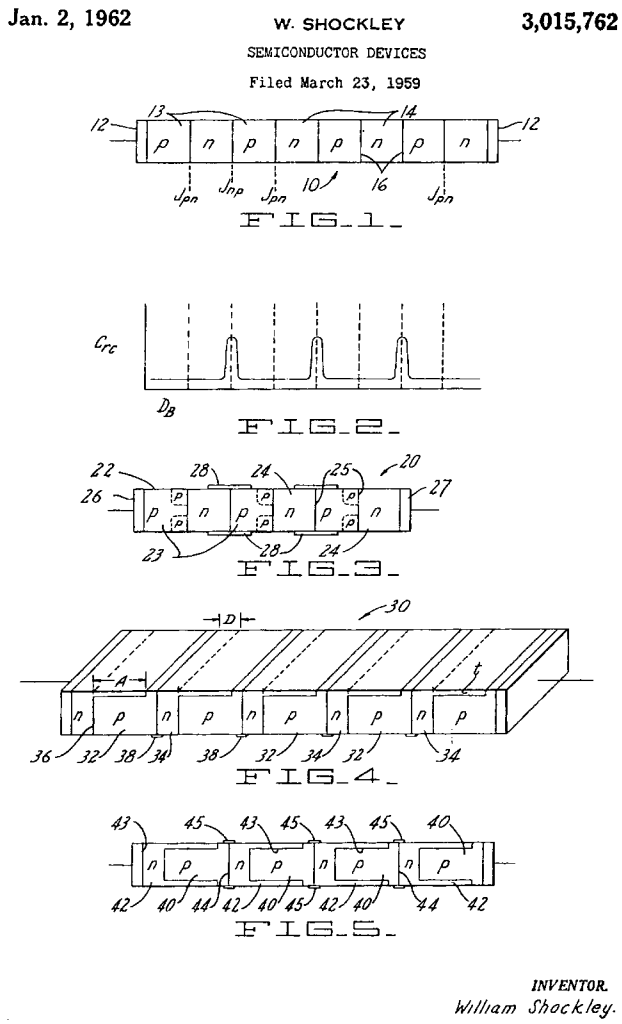


Fig. 27. Shockley's inventive contribution to high-efficiency p-n junction solar battery design (U.S. Patent 3 015 762).

to the Conception of the Junction Transistor" (Appendix 2, [155]), which provided an authoritative account of the circumstances leading to the creation of the most important electronic device of the twentieth century.

VIII. Shockley's Place in the History of Science and Technology

Shockley was one of a kind, a unique, one-man institution (Fig. 30).

The junction transistor, Shockley's epoch-making invention, ushered in the semiconductor revolution. Eighteen years of his professional life were directly spent in the research, development, and commercialization work on transistors. Shockley's decision to go to California to commercialize his inventions and the commercial potential of the junction transistor together created what is now popularly known as Silicon Valley in the San Francisco Bay area.

Shockley's uncanny ability to recognize talent in others, finding the best in people and engaging them in semiconductor research and development, has made a lasting contribution to the accelerated progress of the semiconductor revolution and left his distinct mark long beyond his active involvement in the arena.

From his final years (1935–1936) at MIT, Shockley knew Bardeen and recognized his talent and training in electrical engineering and physics. When Shockley was appointed head of the semiconductor physics group at BTL in September 1945, one of his first acts was to invite and recruit Bardeen to his group. Working on Shockley's field-effect amplifier problem, Bardeen came up with the surface-state theory to explain the problems involved. His collaboration with the experimentalist Brattain quickly led to the unexpected experimental discovery of the point-contact transistor. Working slightly more than two years on an important problem given him by Shockley, Bardeen made a pivotal contribution leading to the discovery of the point-contact transistor, which won him the first Nobel Prize in physics.

In life, being intelligent is not always enough; being there is often of paramount importance. Bardeen gratefully

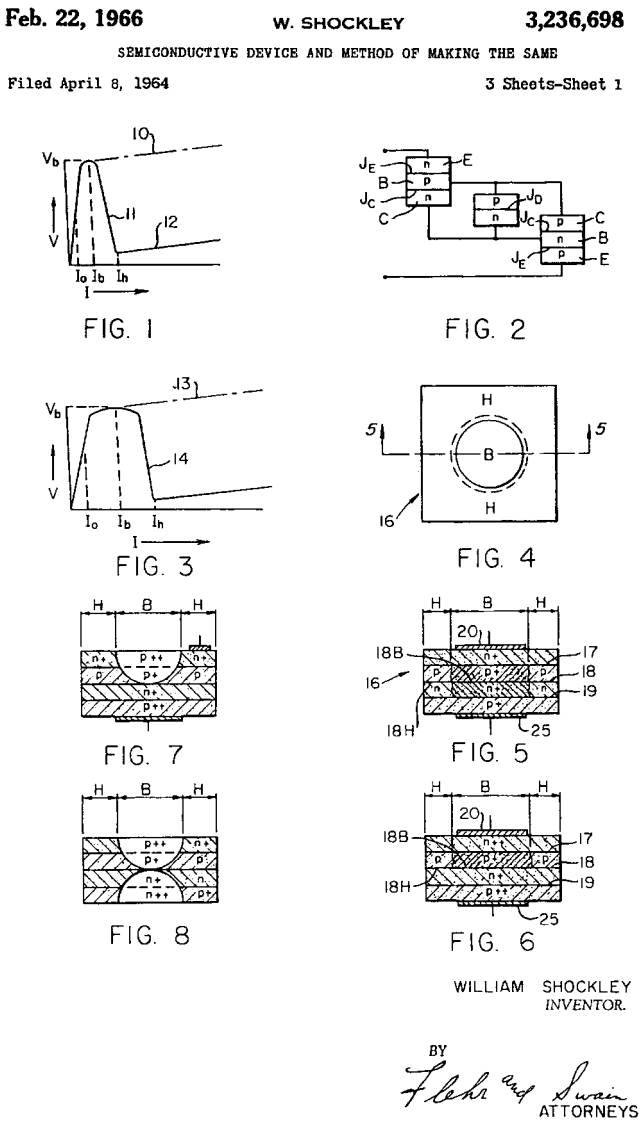


Fig. 28. Shockley's inventive contribution to the improvement of operating characteristics of the p-n-p-n four-layer switching diode (U.S. Patent 3 236 698).

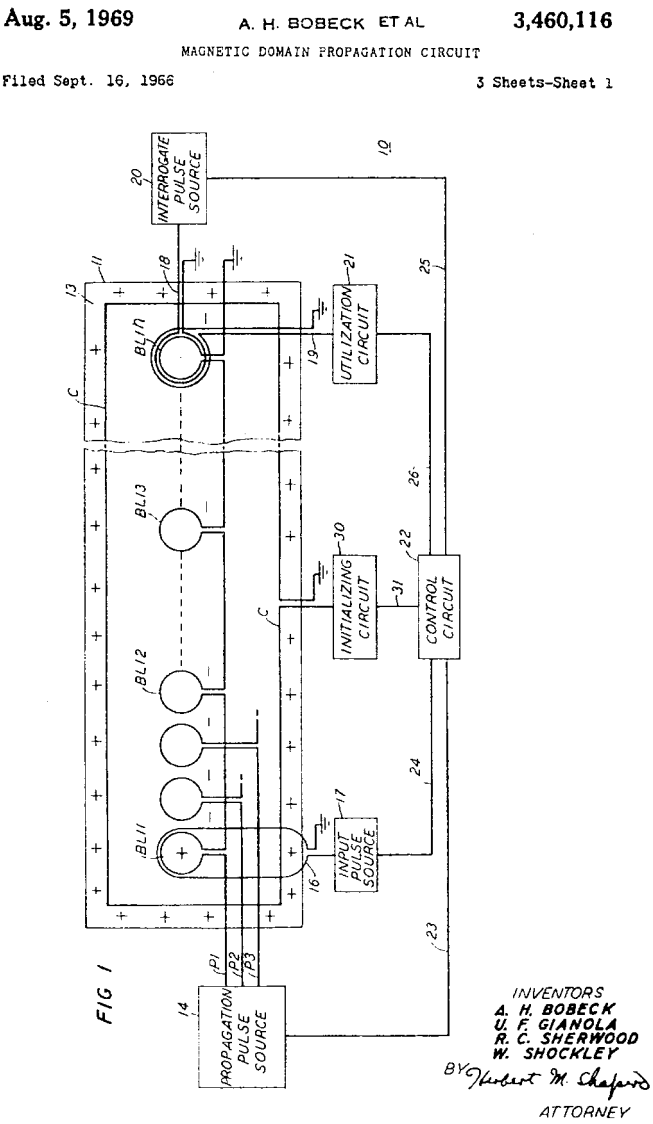


Fig. 29. Shockley's inventive contributions to the design of magnetic thin-film shift registers (U.S. Patent 3 460 116).

remembered Shockley's contribution to his career. In their final salute to Shockley, the Bardeens wrote:

> The years at Bell Labs when John worked closely with Bill were among the most exciting and productive of our lives.
>
> His memory will live on as one of the great scientists of our age.

In Japan, after the devastation of the Second World War came the time for reconstruction and rejuvenation. The invention of the junction transistor right after World War II signalled the arrival of a new technological revolution. The Sony Corporation bought the license from Western Electric (the manufacturing arm of BTL) for $25 000 and began manufacturing junction transistors, applying them to radios and television sets, transforming, and growing rapidly into a giant electronics firm. Its formidable presence in the consumer and entertainment electronics arena is felt from every corner of the globe. We will let Sony's founder and honorary chairman, M. Ibuka, then have the last word on the scientist from whom it all originated:

> We, those who are involved in electronics industry, are all deeply indebted to him for his great invention of the transistor, which made possible today's electronics industry. Without his achievements, today's world may have been totally different. We shall always remember and appreciate his devotion to the whole industry.

Appendix 1
Shockley Patents

[1] W. Shockley, "Electron discharge device," U.S. Patent 2 207 355, July 9, 1940.
[2] ——, "Electron discharge device," U.S. Patent 2 236 012, Mar. 25, 1941.
[3] J. R. Pierce and W. Shockley, "Electron multiplier," U.S. Patent 2 245 605, June 17, 1941.
[4] W. Shockley, "Electron discharge device," U.S. Patent 2 245 614, June 17, 1941.
[5] W. Shockley and G. W. Willard, "Wave propagation device," U.S. Patent 2 407 294, Sept. 10, 1946.

Fig. 30. In him lies the genesis of the San Francisco silicon story [9].

[6] W. Shockley, "Ultra high frequency electronic device," U.S. Patent 2 409 227, Oct. 15, 1946.
[7] ____, "Pulse generator," U.S. Patent 2 416 718, Mar. 4, 1947.
[8] G. L. Pearson and W. Shockley, "Semiconductor amplifier," U.S. Patent 2 502 479, Apr. 4, 1950.
[9] W. Shockley, "Semiconductor amplifier," U.S. Patent 2 502 488, Apr. 4, 1950.
[10] ____, "Differential altimeter," U.S. Patent 2 509 889, May 30, 1950.
[11] ____, "Acoustic transducer utilizing semiconductors," U.S. Patent 2 553 491, May 15, 1951.
[12] ____, "Circuit element utilizing semiconductive materials," U.S. Patent 2 569 347, Sept. 25, 1951.
[13] J. R. Haynes and W. Shockley, "Semiconductor signal translating device with controlled carrier transit times," U.S. Patent 2 600 500, June 17, 1952.
[14] W. Shockley, "Circuit element utilizing semiconductive materials," U.S. Patent 2 623 102, Dec. 23, 1952.
[15] W. Shockley and M. Sparks, "Semiconductor translating device having controlled gain," U.S. Patent 2 623 105, Dec. 23, 1952.
[16] W. Shockley, "Semiconductor signal translating device," U.S. Patent 2 654 059, Sept. 29, 1953.
[17] ____, "Bistable circuits including transistors," U.S. Patent 2 655 609, Oct. 13, 1953.
[18] ____, "Semiconductor translating device," U.S. Patent 2 666 814, Jan. 19, 1954.
[19] ____, "Transistor amplifier," U.S. Patent 2 666 818, Jan. 19, 1954.
[20] ____, "Semiconductor translating device," U.S. Patent 2 672 528, Mar. 16, 1954.
[21] ____, "Circuit element utilizing semiconductive materials," U.S. Patent 2 681 993, June 22, 1954.
[22] H. B. Briggs, J. R. Haynes, and W. Shockley, "Infrared energy source," U.S. Patent 2 683 794, July 18, 1954.
[23] W. Shockley, "Electrooptical control system," U.S. Patent 2 696 565, Dec. 7, 1954.
[24] ____, "Circuits, including semiconductor device," U.S. Patent 2 714 702, Aug. 2, 1955.
[25] ____, "Transistor circuits with constant output current," U.S. Patent 2 716 729, Aug. 30, 1955.
[26] ____, "Method of making semiconductor crystals," U.S. Patent 2 730 470, Jan. 10, 1956.
[27] ____, "Semiconductor signal translating devices," U.S. Patent 2 744 970, May 8, 1956.
[28] ____, "Semiconductor signal translating devices," U.S. Patent 2 756 285, July 24, 1956.
[29] ____, "Frequency selective semiconductor circuit elements," U.S. Patent 2 761 020, Aug. 28, 1956.

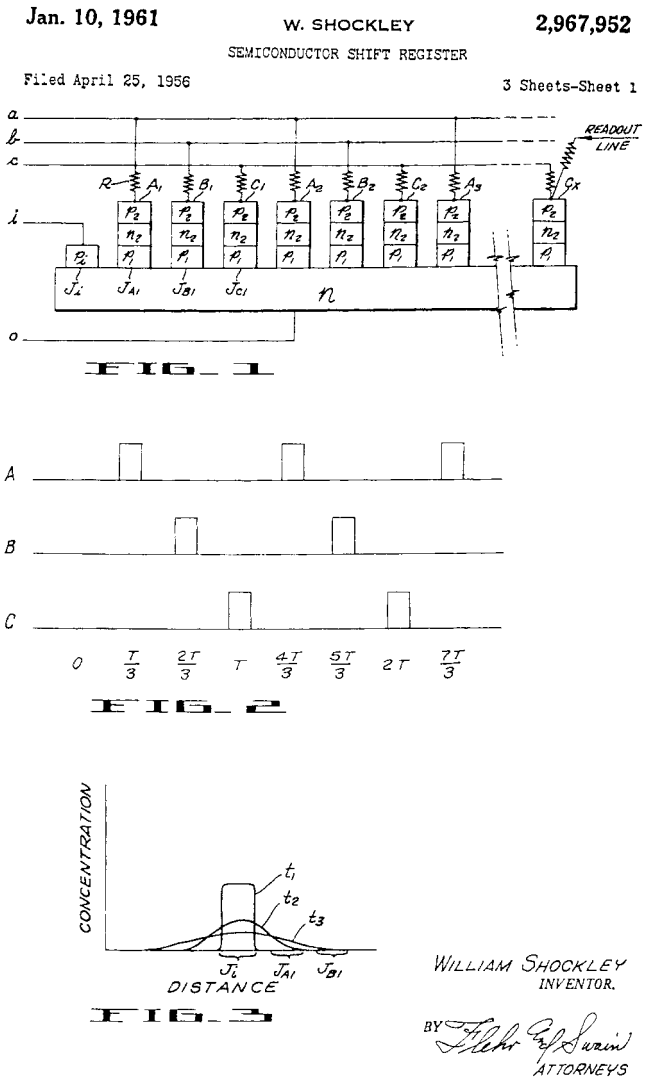


Fig. 31. Semiconductor shift register patent.

[30] ____, "Semiconductor circuit controlling device," U.S. Patent 2 763 832, Sept. 18, 1956.
[31] ____, "Semiconductor signal translating devices," U.S. Patent 2 764 642, Sept. 25, 1956.
[32] ____, "Negative resistance device application," U.S. Patent 2 772 360, Nov. 27, 1956.
[33] W. P. Mason and W. Shockley, "Negative resistance amplifiers," U.S. Patent 2 775 658, Dec. 25, 1956.
[34] W. Shockley, "Asymmetric waveguide structure," U.S. Patent 2 777 906, Jan. 15, 1957.
[35] ____, "Semiconductor signal translating devices," U.S. Patent 2 778 885, Jan. 22, 1957.
[36] ____, "Forming semiconductive devices by ionic bombardment," U.S. Patent 2 787 564, Apr. 2, 1957.
[37] ____, "Semiconductor signal translating devices," U.S. Patent 2 790 037, Apr. 23, 1957.
[38] ____, "Nonreciprocal circuits employing negative resistance elements," U.S. Patent 2 794 864, June 4, 1957.
[39] ____, "High frequency negative resistance device," U.S. Patent 2 794 917, June 4, 1957.
[40] ____, "Semiconductive device," U.S. Patent 2 813 233, Nov. 12, 1957.
[41] ____, "Method of fabricating semiconductor signal translating devices," U.S. Patent 2 816 847, Dec. 17, 1957.
[42] ____, "High frequency negative resistance device," U.S. Patent 2 852 677, Sept. 16, 1958.
[43] ____, "Semiconductive switch," U.S. Patent 2 855 524, Oct. 7, 1958.
[44] ____, "Method of forming large area P-N junctions," U.S. Patent 2 868 678, Jan. 13, 1959.

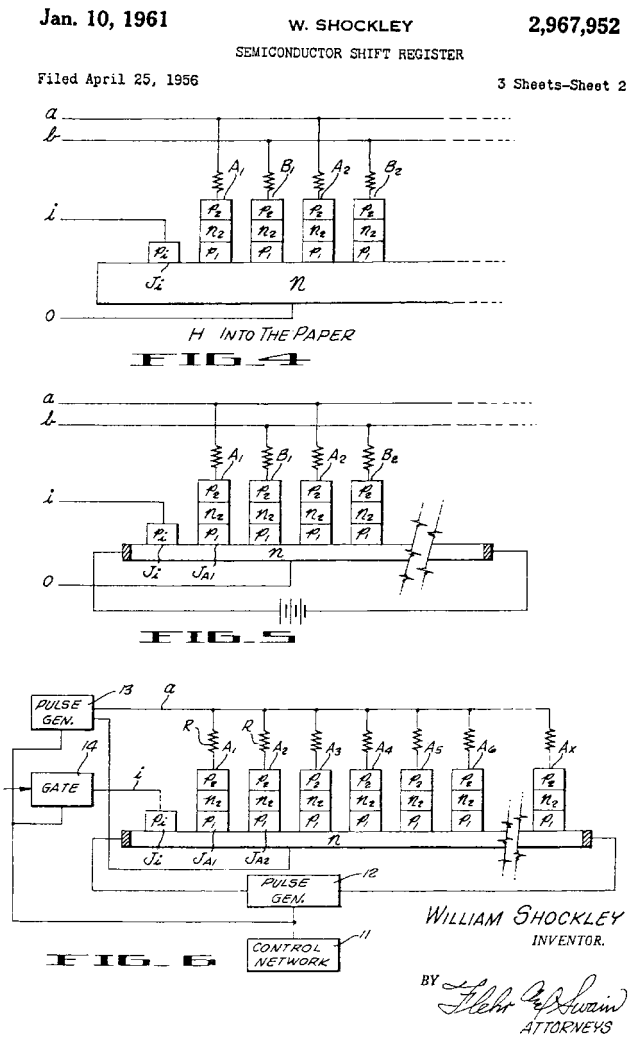


Fig. 31. *(Continued.)* Semiconductor shift register patent.

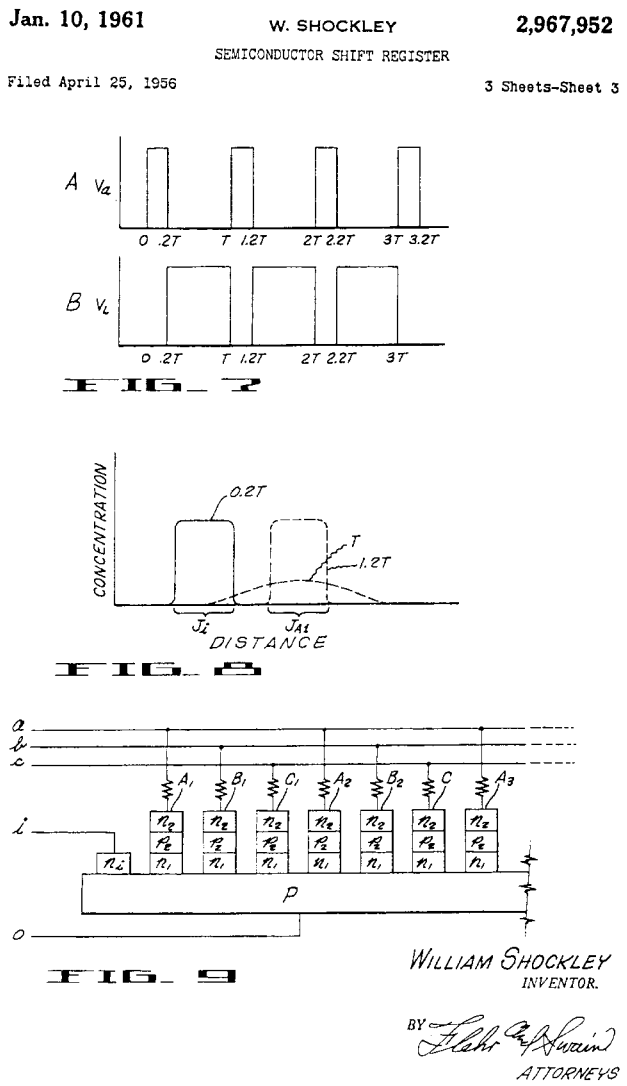


Fig. 31. *(Continued.)* Semiconductor shift register patent.

[45] ____, "Negative resistance semiconductive device," U.S. Patent 2 869 084, Jan. 13, 1959.
[46] ____, "Method for growing junction semiconductive devices," U.S. Patent 2 879 189, Mar. 24, 1959.
[47] ____, "Radiant energy control system," U.S. Patent 2 884 540, Apr. 28, 1959.
[48] ____, "Semiconductive material purification method and apparatus," U.S. Patent 2 890 139, June 9, 1959.
[49] ____, "Transistor switch," U.S. Patent 2 891 171, June 16, 1959.
[50] ____, "Shifting register," U.S. Patent 2 912 598, Nov. 10, 1959.
[51] ____, "Crystal growing apparatus," U.S. Patent 2 927 008, Mar. 1, 1960.
[52] ____, "Semiconductor amplifying device," U.S. Patent 2 936 425, May 10, 1960.
[53] ____, "Semiconductive device and method," U.S. Patent 2 937 114, May 17, 1960.
[54] ____, "P-N junction having minimum transition layer capacitance," U.S. Patent 2 953 488, Sept. 20, 1960.
[55] ____, "Grain boundary semiconductor device and method," U.S. Patent 2 954 307, Sept. 27, 1960.
[56] ____, "Semiconductor shift register," U.S. Patent 2 967 952, Jan. 10, 1961.
[57] W. Shockley and R. N. Noyce, "Transistor structure," U.S. Patent 2 967 985, Jan. 10, 1961.
[58] W. Shockley and R. V. Jones, "Crystal growing apparatus," U.S. Patent 2 979 386, Apr. 11, 1961.
[59] W. Shockley, "Semiconductor device and method of making the same," U.S. Patent 2 979 427, Apr. 11, 1961.
[60] ____, "Junction transistor," U.S. Patent 2 980 830, Apr. 18, 1961.
[61] ____, "Fabrication of semiconductor elements," U.S. Patent 2 982 002, May 2, 1961.
[62] ____, "Method of making a semiconductive switching array," U.S. Patent 2 994 121, Aug. 1, 1961.
[63] ____, "Semiconductive device and method of operating same," U.S. Patent 2 997 604, Aug. 22, 1961.
[64] ____, "Semiconductor devices," U.S. Patent 3 015 762, Jan. 2, 1962.
[65] G. C. Dacey, C. A. Lee, and W. Shockley, "Semiconductive device and method of operating same," U.S. Patent 3 028 655, Apr. 10, 1962.
[66] W. Shockley, "Process for growing single crystals," U.S. Patent 3 031 275, Apr. 24, 1962.
[67] ____, "Semiconductive wafer and method of making the same," U.S. Patent 3 044 909, July 17, 1962.
[68] ____, "Reverse breakdown diode pulse generator," U.S. Patent 3 048 710, Aug. 7, 1962.
[69] ____, "Method of growing silicon carbide crystals," U.S. Patent 3 053 635, Sept. 11, 1962.
[70] ____, "Trigger circuit switching from stable operation in the negative resistance region to unstable operation," U.S. Patent 3 058 009, Oct. 9, 1962.
[71] ____, "Electrical component holder," U.S. Patent 3 076 170, Jan. 29, 1963.
[72] W. Shockley and A. Goetzberger, "Thermostat," U.S. Patent 3 079 484, Feb. 26, 1963.
[73] W. Shockley and A. O. Beckman, "Semiconductor leads and method of attaching," U.S. Patent 3 086 281, Apr. 23, 1963.
[74] W. Shockley, "Method of making thin slices of semiconductive material," U.S. Patent 3 096 262, July 2, 1963.
[75] ____, "Semiconductive device," U.S. Patent 3 099 591, July 30, 1963.

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2,967,952

SEMICONDUCTOR SHIFT REGISTER

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This invention relates generally to shift registers and more particularly to a semiconductor shift register.

It is an object of the present invention to provide a novel semiconductor shift register.

It is another object of the present invention to provide a semiconductor shift register which operates in response to controlling pulses.

It is another object of the present invention to provide a semiconductor shift register which includes a common region of semiconductive material having a plurality of semiconductor devices forming junctions therewith.

It is still another object of the present invention to provide a semiconductor shift register which includes a common semiconductive body of one conductivity type having a plurality of devices each including outer regions of opposite conductivity type and an intermediate region of the same conductivity type forming junctions therewith.

It is a further object of the present invention to provide a semiconductor shift register which includes a common semiconductive body having a plurality of devices each including outer regions of opposite conductivity type and an intermediate region of the same conductivity type forming junctions therewith and in which said devices are spaced from one another whereby diffusion of injected carriers serves to bias adjacent junctions.

It is still a further object of the present invention to provide a shift register which is inexpensively and easily manufactured and which is efficient and economical to operate.

The invention possesses other objects and features of advantage, some of which with the foregoing will be set forth in the following description of the invention. It is to be understood that the invention is not to be limited to the disclosure of the species of the invention described, as other embodiments thereof may be adopted within the scope of the claims.

Referring to the drawings:

Figure 1 is a schematic diagram representing one embodiment of the invention;

Figures 2A–2C show typical pulses employed to operate the shift register of Figure 1;

Figure 3 is a graph of concentration of carriers as a function of distance for various times;

Figure 4 is a view illustrating an embodiment of the invention in which two devices form a storage unit and in which a magnetic field serves to deflect injected carriers;

Figure 5 is a view illustrating an embodiment of my invention in which two devices form a storage unit and in which a longitudinal electric field serves to deflect the injected carriers;

Figure 6 is a view illustrating an embodiment of my invention in which a single device forms a storage unit and in which a pulse longitudinal electric field serves to deflect injected carriers;

Figures 7A—7B show typical pulses employed to operate the register of Figure 6;

Figure 8 is a graph of concentration of carriers for various times; and

Figure 9 illustrates still another embodiment of my invention.

Referring to Figure 1, the semiconductor shift register illustrated comprises an n-type body of semiconductive material having a plurality of semiconductive devices (islands) A_1, B_1, C_1, A_2, B_2, C_2, etc., contiguous therewith to form a plurality of junctions. The devices illustrated each have an n-type region n_2 which is intermediate the p-type regions p_1 and p_2. It is, of course, to be understood that the body may be formed of p-type semiconductive material with the plurality of devices (islands) each having n-p-n type regions, as illustrated in Figure 9.

Any suitable semiconductive material may be employed to form the shift register. For example, the body may be germanium or silicon to which is added impurities to form the proper conductivity type. Suitable layers of different conductivity types are formed on the body and the resulting block is cut mechanically, electrically or electrochemically to form suitable devices (islands) of the type described.

For example, to form the register shown in Figure 1, donor impurities may be added to pure germanium or silicon to form the body. Employing diffusion techniques, a p-type layer (region) is formed on the upper surface of the n-type semiconductive body. A layer of n-type semiconductive material is then formed on the p-type layer, and a third layer of p-type material is then formed on the n-type layer. This forms an n-type body having layers (regions or strata) of p-type, n-type, and p-type material on one surface. The block of material thus formed can then be cut into strips and machined to form the devices A_1, B_1, etc., as shown in Figure 1. A p_1 region is then diffused into the n-type common region to form the junction J_1.

The register formed as described will then include a plurality of devices (islands) A_1, B_1, etc. which are adjacent to one another and which form junctions J_{A1}, J_{B1}, etc. with the n-type body. The spacing between the devices will depend upon the diffusion rate of injected minority carriers in the common semiconductive region, the lifetime and concentration of the carriers, and the cycle rate of the register, as will be presently described.

A triggering or switching semiconductor device which will be triggered in response to a predetermined triggering voltage may be formed with four regions, n-p-n-p. A device of this type will trigger from a low conducting (high resistance) to a high conducting (low resistance) state in response to a voltage having a predetermined amplitude. The voltage across the device is applied with a polarity which serves to bias the end junctions in a forward direction and to reversely bias the center junction. The device may then be viewed as a pair of complementary transistors with the center junction acting as the collector of each. As the voltage is increased, avalanche sets in at the center (collector) junction. The current increases rapidly. If means are provided whereby the complementary transistors have low alphas for low current densities and high alphas for high current densities, then when avalanche sets in the sum of the alphas for the two transistors will be greater than one and the device will make a rapid transition to the high conductance condition. The voltage required to sustain conduction will be considerably less than the voltage required to trigger or switch the device.

It is apparent upon a study of the shift register shown in Figure 1 that each of the devices A_1, B_1, C_1, etc. may be considered an n-p-n-p semiconductor device. By placing the devices or islands near one another, carriers injected into the body at the junction formed therewith will

Fig. 31. *(Continued.)* Semiconductor shift register patent.

[76] ____, "Field effect transistor having grain boundary therein," U.S. Patent 3 126 505, Mar. 24, 1964.
[77] W. Shockley and R. N. Noyce, "Method of making a transistor structure," U.S. Patent 3 140 206, July 7, 1964.
[78] W. Shockley and G. S. Horseley, "Voltage regulating semiconductor device," U.S. Patent 3 140 438, July 7, 1964.
[79] W. Shockley, "Voltage regulating semiconductor device," U.S. Patent 3 154 692, Oct. 27, 1964.
[80] G. C. Dacey, C. A. Lee, and W. Shockley, "Mesa transistor with impurity concentration in the base decreasing toward collector junction," U.S. Patent 3 202 887, Aug. 24, 1965.
[81] W. Shockley, "Semiconductive device and method of making the same," U.S. Patent 3 236 698, Feb. 22, 1966.

spread by diffusion to adjacent junctions. These carriers diffuse across the adjacent junctions and serve to bias the same in a forward direction. The emitter current and the currents flowing across the junctions (emitter and central junctions) is increased. As previously described, the alpha of the junction increases with current.

With sufficient bias the alphas increase whereby the device is biased into a conducting state. Application of a voltage considerably less than the voltage required to switch or trigger an unbiased n-p-n-p device will cause the device to conduct large currents.

Referring to Figure 1 again, a pulse which applies forward bias to the junction J_1 will serve to inject holes into the n-type body. The injected holes (carriers) spread by diffusion in a manner which is illustrated in the graph of Figure 3. This graph shows carrier concentration as a function of distance for various times. The concentration of carriers adjacent the junction J_1 is shown by the curve t_1 immediately after application of the pulse to line *i*. A short interval of time later, the distribution is shown by the curve t_2. The carriers have spread by diffusion in both directions from the junction J_1, some of the carriers having diffused as far as the junction J_{A1}. At the time t_3, more spread has taken place and more carriers are adjacent the junction J_{A1} with a few of the carriers having diffused as far as the junction J_{B1}. Recombination is taking place in the n-type region and the total number of carriers is decreasing with time.

Minority carriers in the vicinity of the junction J_{A1} diffuse into the p_1 region where they provide a forward bias for the junction, as previously described. This forward bias improves the alpha of the pair of junctions. If the bias is sufficient to increase the alphas of the device A_1 so that their sum is greater than one, the device will trigger in the conducting state and will carry large currents for a pulse having an amplitude less than the switching voltage required for an n-p-n-p device.

It is apparent that the pulse (Figure 2A) must be applied to the line *a* at a predetermined time interval after the application of the pulse at the line *i*, the time depending upon the diffusion, recombination and concentration of minority carriers. Preferably, the various devices (islands) are spaced as close as possible to one another whereby the carriers rapidly diffuse over to the adjacent junction to bias the same. This increases the speed of operation of the register, since the carriers have to diffuse a lesser distance to bias the adjacent junction. The time lapse required between the input pulse and the application of a shifting or control pulse to the line *a* may be controlled by controlling the diffusion constant of the body, by controlling the spacing between the various devices (islands), and by controlling the magnitude of the pulse applied to the line *i* (the concentration of minority carriers).

Referring again to Figure 1, driving lines *a*, *b* and *c* are connected to the devices A, B and C respectively through current limiting resistors R. By application of pulses sequentially to the lines *a*, *b* and *c*, the register serves to shift bits of information introduced on the line *i*, as will be presently described. In the embodiment shown in Figure 1, each storage cell which serves to store a bit of information comprises three devices A, B and C. Thus, devices A_1, B_1 and C_1 form one storage cell, A_2, B_2 and C_2, another storage cell, etc.

Referring to Figures 1, 2 and 3, operation of the device is as follows: Consider, for example, the condition where a pulse is applied to the line *i*, causing injection of holes into the n-type body. At the time $T/3$, the carriers which have diffused to the junction J_{A1} have reached approximately their maximum concentration. If the pulse (Figure 2A) which has an amplitude less than the switching voltage for an unbiased device is applied to the line *a*, the device A_1 will carry a current limited by the series resistor R. The pulse on line *a* will not cause devices A_2, A_3 etc. to switch since the amplitude of the pulse is less than the switching voltages for the devices. The junctions J_{A2} and J_{A3} are sufficiently removed from the junction J_1 that no carriers will diffuse to these junctions to bias the same into the conducting state. When the device A_1 switches into a conducting condition, the p_1 region will inject carriers (in this case, holes) into the n-type body. The carriers injected by the device A_1 will diffuse toward the junctions J_1 and J_{B1} and J_{C1}.

If, at a predetermined time later, time $2T/3$, a pulse is applied to the line *b*, the device B_1 will switch into a conducting state; devices B_2 etc. will not be switched since they are not sufficiently biased by injected minority carriers. The time lapse between the injection of carriers by the device A_1 and the application of a voltage pulse to the line *b* is dependent upon the spacing of the devices, the density of the injected carriers, and the diffusion and recombination rates of the n-type body, as has been previously described. The device B_1 injects carriers into the n-type body. The carriers diffuse toward the junctions J_{C1}, J_{A2}, etc. and toward the junctions J_{A1} and J_1. A pulse applied to either the line *a* or *c* will cause the respective devices A_1 or C_1 to become conducting. In order for the wave to travel forward, the line *c* is energized at time T, thereby switching the device C_1 into a conducting state. The device C_1 will then inject carriers as previously described, which will serve to spread by diffusion to adjacent junctions.

It is apparent that during the period of time 0–T, the devices A_2, B_2, and C_2 have not been switched into a conducting state, since the amplitude of the voltage pulses applied did not exceed the breakdown voltage for the devices, and none of the devices were biased by diffusing minority carriers.

Application of a pulse to line *a* at time $4T/3$ will cause device A_2 to become conducting. If the carriers are injected in great quantities, they may diffuse back to A_1 where application of a pulse at $4T/3$ will cause it to become conducting regardless of whether or not a pulse was applied to line *i*. In such event, the amplitude of the pulses may be reduced or the values of the resistors increased. The concentration will then be such that they will die out in the time T whereby they will be ineffective in supporting a backward wave.

It is convenient to represent digital information representing "1" by conduction and information representing "0" by non-conduction. A new bit of information representing "1" should be introduced to the line *i* at the instant line *c* is pulsed. Thus, if a "1" is introduced at time 0, T, 2T, etc., a conducting state will be generated and transferred from device to device along the series progressing from *i* to C_1 in time T and from C_1 to C_2 in an additional time T, etc. On the other hand if an "0" is introduced by not pulsing *i* at any of the times 0, T, 2T, etc., then the "0" will be transmitted in the form of a non-conducting state from *i* to C_1 in a time T, etc.

It is apparent that three devices are necessary to make up a storage unit of the shift register illustrated in Figure 1, each of the units serving to store one bit of information. One cycle is represented by the time 0–T which represents pulses applied successively to the lines *a*, *b* and *c*. In the foregoing example, the information originally stored in the first storage unit comprising devices A_1, B_1, and C_1, has been shifted to the second storage unit comprising the devices A_2, B_2 and C_2 in the time T.

Suitable circuits may be employed for gating the information to the line *i* whereby the information is applied simultaneously with the application of pulses to the line *c*.

The information in the shift register may be held stationary by repeatedly pulsing one of the lines without pulsing the others. Under these conditions, each conducting device will reactivate itself, but the spread of carriers from one device to the next one of the same type, i.e., from one A device to another A device, cannot occur since the distance is three times the distance between elements and the register is so designed that adequate transmission

Fig. 31. *(Continued.)* Semiconductor shift register patent.

[82] ____, "Thermally stabilized semiconductor device," U.S. Patent 3 286 138, Nov. 15, 1966.

[83] ____, "Surface controlled avalanche transistor," U.S. Patent 3 339 086, Aug. 29, 1967.

[84] W. Shockley and R. H. Haitz, "Noise diodes," U.S. Patent 3 349 298, Oct. 24, 1967.

[85] W. Shockley and D. R. Curran, "Piezoelectric resonator," U.S. Patent 3 384 768, May 21, 1968.

[86] W. Shockley, "Semiconductor device having regions of different conductivity types wherein current is carried by the same type of carrier in all said regions," U.S. Patent 3 398 334, Aug. 20, 1968.

of carriers is only produced between an element and the next adjacent element, as previously described.

It is, of course, apparent that by controlling the sequence in which the lines are pulsed the information may be transferred in either direction, as desired. For example, if line *b* is pulsed after line *c*, the information will travel to the left, as represented by Figure 1, rather than to the right.

The information may be read serially from the register by applying a pulse to the readout line associated with the last device C_x simultaneously with the pulsing of the line *c*. If the device C_x is conducting (representing "1"), a high current will flow whereas if the device C_x is non-conducting (representing "0"), no current will flow. Of course, if it is desirable, the information may be read out of any one of the devices by pulsing the device at the appropriate time. The information may also be obtained in parallel by pulsing any one of the devices A, B or C of each of the storage units as the respective line *a*, *b* or *c* is pulsed.

The shift register illustrated in Figure 1 requires three devices to form a storage unit or cell in order that information be transferred in one direction. In the embodiment illustrated in Figure 4, two devices form each storage unit or cell. The device illustrated includes devices A_1, B_1, A_2, B_2, etc. which are connected to driving lines *a* and *b* through the resistors R. A suitable junction for injecting carriers is formed at J_1. As before, the information is suitably gated to the line *i* whereby carriers are injected into the n-type body. As in the previous example, by pulsing the line *a*, a suitable time subsequent thereto, when the carriers have attained the approximate maximum concentration in the adjacent junction J_{A1} to bias the same into a conducting state, the device A_1 will carry a current limited by the associated resistance. In the previous example, the carriers spread by diffusion in all directions, as illustrated in Figure 3. In the example shown in Figure 4, a transverse magnetic field H, having a direction into the paper, for the example illustrated, is applied to the device. A relatively large number of the carriers which are injected by the p_1 region are deflected to the right to bias the junction J_{A1}. Similarly, relatively large numbers of carriers injected by the devices (islands) A_1, B_1, A_2, B_2, etc. will be deflected to the right to bias the junctions to the right, while relatively few of the carriers will diffuse to the left. Two devices suffice to form a storage unit. New information representing "1" may be introduced at the instant the line *b* is pulsed, whereby upon a subsequent application of a pulse to line *a*, the device A_1 will become conducting. If a pulse is not applied to the line *a*, the device A_1 will not become conducting, since, because of the magnetic field, few of the carriers injected by B_1 diffuse to J_{A1}.

Information may be transferred to the left by reversing the magnetic field, thus deflecting the carriers in the opposite direction. In all other respects, the device operates as the devices shown in Figure 1. Thus, the information may be removed serially at the end or in parallel from either one of the switching devices A or B of each cell. The information may be stored in a particular storage unit by repeatedly pulsing one of the lines.

Another shift register in which each of the storage elements comprises two switching devices is shown in Figure 5. In this embodiment, a relatively large number of the carriers which are injected are deflected to the right by means of a longitudinal electric field. Again, to reverse the direction of shifting of the information, the electric field is reversed.

In certain applications where a longitudinal electric field is employed, it may be desirable to make the body of semiconductive material very thin so as to reduce heating. This may be accomplished without loss of mechanical strength by forming the body of material as a thin layer of the requisite conductivity type on the surface of a more massive body of the opposite conductivity type. Electrical separation can be effectively produced and maintained by reversely biasing the resulting junction. Various means are well known for producing such layers. For example, impurities may be diffused from the outside, or a p-n junction may be grown from a melt and cut.

Figure 6 illustrates a shift register in which each of the storage units which serves to store a bit of information comprises a single device or island. A pulsed longitudinal electric field is employed to shift the information. Referring to Figure 7, suitable voltages are shown for operating the register. Thus a pulse is applied to the line *a* which has a short duration, for example, as shown 0–0.2T. A pulsed longitudinal voltage V_L is then applied. As illustrated in Figure 7B, the longitudinal voltage pulse has a duration of approximately .8T extending from point 0.2T to T. Holes injected during the time 0 to 0.2T build up a high concentration below the junction J_1 as shown in Figure 8. The pulsed longitudinal electric field is then applied and causes the hole concentration to drift along the common body. After approximately 0.8T, holes have been displaced and are adjacent the device A_1 where they serve to bias the junction J_{A1}. As previously described, this serves to bias the associated device into a conducting state whereupon application of a pulse to line *a* causes a large current limited by the associated resistor R to flow through the device. Application of the next pulse to the line *a* will serve to inject holes at the device A_1 at 1.2T of Figure 8. The next longitudinal pulse will transfer the holes to the junction J_{A2}, etc.

The period T, the duration of the injection and the longitudinal pulses, and the magnitudes of the injection and the longitudinal pulses may be adjusted whereby the highest injected carrier density produced by one pulse will be found one unit to the right of the point of injection at the instant of application of the next pulse to line *a*. It is apparent that this will produce a transfer of bits of information with only one device being used to store each bit.

One advantage of pulsing the longitudinal field is that it moves the injected carriers after injection, rather than spreading them during injection. Another advantage is that it leaves the main body of material at one potential when a pulse is applied to the line *a*.

A control network **11** may be employed to control the operation of the longitudinal or sweeping pulse generator **12**, the injection pulse generator **13**, and the gate **14**.

If the duration of the injection pulse is short compared to the time required to drift from one device to the next, a D.-C. field may be used provided, however, that the voltage wave on line *a* produces a distribution of voltages along the device which swings all of the junctions J_{A1}, J_{A2}, etc. from forward to reverse bias.

This can be accomplished in a variety of ways, such as connecting the resistor R associated with each device to a point on a voltage divider. It may also be achieved by making the voltage swing large compared to the voltage drop produced by the sweeping field, but small compared to the voltage required to break down the devices.

In Figure 9, a shift register similar to that shown in Figure 1 is illustrated. In this register, the body is of p-type material, rather than n-type material with the devices forming junctions therewith being of the n-p-n-type. It is apparent that this device will operate in a similar manner. The pulses applied will have a polarity opposite to that required for the device of Figure 1. It is apparent that all of the other devices previously described may also be formed of n-p-n type with a common base of p-type material.

The operation of the devices shown in Figures 1–9 may be enhanced by applying substantial reverse voltages between pulses whereby the devices are rapidly triggered into a non-conducting state.

Thus it is seen that I have provided a novel semiconductor shift register which serves to shift informa-

Fig. 31. *(Continued.)* Semiconductor shift register patent.

[87] A. H. Bobeck, U. F. Gianola, R. C. Sherwood, and W. Shockley, "Magnetic domain propagation circuit," U.S. Patent 3 460 116, Aug. 5, 1969.

[88] A. H. Bobeck, P. C. Michaelis, and W. Shockley, "Readout implementation for magnetic memory," U.S. Patent 3 508 222, Apr. 21, 1970.

[89] A. H. Bobeck, H. E. D. Scovil, and W. Shockley, "Magnetic logic arrangement," U.S. Patent 3 541 522, Nov. 17, 1970.

[90] J. A. Davis and W. Shockley, "Chopper devices and circuits," U.S. Patent 3 808 515, Apr. 30, 1974.

APPENDIX 2
SHOCKLEY PAPERS

[1] R. P. Johnson and W. Shockley, "An electron microscope for filaments: Emission and absorption by tungsten single crystals,"

tion in response to control pulses. The register is inexpensive and easy to manufacture, and economical and reliable in operation.

I claim:

1. A semiconductor shift register comprising a body of semiconductor material, a plurality of semiconductor devices forming a junction with said body, a portion of said body forming a region in each device and the junction being a junction in the respective device, each of said devices being adapted to be triggered from a low conducting to a high conducting state in response to a pulse having at least a predetermined amplitude and serving to inject carriers into the body when in a high conducting state, the devices being so spaced that the injected carriers diffuse to adjacent devices to bias the same, and said devices being arranged to form storage units each adapted to store a bit of information, means for injecting carriers into said body adjacent the first device in response to information, means for applying controlling pulses across the devices, said pulses having an amplitude which is sufficient to trigger biased devices into a high conducting state but less than the triggering voltage of an unbiased device, said controlling pulses being so timed and applied that they serve to shift the input information to successive devices or store the information, and means connected to at least one device for reading out the information.

2. A semiconductor shift register as in claim 1 wherein each of said devices including the body region includes p-n-p-n conductivity type regions.

3. A semiconductor shift register comprising a body of semiconductor material, a plurality of semiconductor devices forming a junction with said body, a portion of said body forming a region in each device and the junction being a junction in the respective device, each of said devices being adapted to be triggered from a low conducting to a high conducting state in response to pulses having at least a predetermined amplitude and serving to inject carriers into the body when in a high conducting state, the devices being so spaced that injected carriers diffuse to adjacent devices to bias the same, and said devices being arranged in threes to form storage units each adapted to store one item of information, means for injecting carriers into said body adjacent the first device in response to an information pulse, three control lines, alternate control lines being connected to successive ones of said devices with like devices in each of said storage units connected to the same line, means for applying controlling pulses along said lines and across the devices, said pulses having an amplitude which is sufficient to trigger biased devices into a high conducting state but less than the triggering voltage, said pulses having a predetermined timing whereby the information is shifted to successive devices or stored, and means connected to at least one device for reading out the information.

4. An apparatus as in claim 3 wherein each of said devices including the body region includes p-n-p-n conductivity type regions.

5. A semiconductor shift register comprising a body of semiconductor material, a plurality of semiconductor devices forming a junction with said body, a portion of said body forming a region in each device and the junction being a junction in the device, each of said devices being adapted to be triggered from a low conducting to a high conducting state in response to a pulse having at least a predetermined amplitude and to inject carriers into the body when in a high conducting state, said devices being so spaced and arranged that injected carriers diffuse to adjacent devices to bias the same, an adjacent pair of said devices forming a storage unit adapted to store information, means for injecting carriers into said body adjacent the first device in response to information, a pair of lines alternately connected to successive ones of said devices, means for applying controlling pulses to said lines across said devices, said pulses having an amplitude which is sufficient to trigger biased devices into a high conducting state but less than the triggering voltage, means for deflecting said injected carriers towards one or the other of the adjacent devices, said pulses having a predetermined timing whereby the information is shifted to successive devices in the direction of deflection of the carriers or stored, and means connected to at least one device for reading out the information.

6. An apparatus as in claim 5 wherein said body is an elongated body having the devices arranged substantially in line along the same and wherein said means for deflecting the carriers comprises an electric field applied longitudinally of said body.

7. Apparatus as in claim 5 wherein said body is an elongated body, and wherein said means for deflecting the carriers comprises a magnetic field applied transverse to the longitudinal axis of said body.

8. Apparatus as in claim 5 wherein each of said devices including the body region includes p-n-p-n conductivity type regions.

9. A semiconductor shift register comprising an elongated body of semiconductor material, a plurality of semiconductor devices forming a junction with said body, a portion of said body forming a region in each device and the junction being a junction in the device, each of said devices being adapted to be triggered from a low conducting to a high conducting state in response to pulses having at least a predetermined amplitude and serving to inject carriers into the body when in a high conducting state, said devices being so arranged that injected carriers diffuse to adjacent devices to bias the same, each of said devices forming a storage unit adapted to store one bit of information, means for injecting carriers into said body adjacent the first device in response to an information pulse, a line connected to each of said devices, means for applying controlling pulses to said line across said devices, said pulses having an amplitude which is sufficient to trigger biased devices into a high conducting state but less than the triggering voltage, and means for applying pulses longitudinally of said body to deflect the carriers longitudinally of said body, said longitudinal and controlling pulses being timed whereby the information is shifted to adjacent devices or stored.

10. Apparatus as in claim 9 wherein each of said devices including the body region includes p-n-p-n conductivity type regions.

References Cited in the file of this patent

UNITED STATES PATENTS

2,553,490	Wallace	May 15, 1951
2,586,080	Pfann	Feb. 19, 1952
2,594,336	Mohr	Apr. 29, 1952
2,600,500	Haynes et al.	June 17, 1952
2,655,607	Reeves	Oct. 13, 1953
2,655,610	Ebers	Oct. 13, 1953
2,663,806	Darlington	Dec. 22, 1953
2,663,830	Oliver	Dec. 22, 1953
2,689,930	Hall	Sept. 21, 1954
2,735,948	Sziklai	Feb. 21, 1956
2,756,285	Shockley	July 24, 1956
2,770,740	Reeves et al.	Nov. 13, 1956
2,790,037	Shockley	Apr. 23, 1957
2,856,544	Ross	Oct. 14, 1958
2,877,358	Ross	Mar. 10, 1959

Fig. 31. *(Continued.)* Semiconductor shift register patent.

Phys. Rev., vol. 49, pp. 436–440, Mar. 15, 1936.

[2] W. Shockley, "Application of an electrical timing device to certain mechanics experiments," *Amer. Phys. Teacher*, vol. 4, pp. 76–81, May 1936.

[3] J. C. Slater and W. Shockley, "Optical absorption by the alkali halides," *Phys. Rev.*, vol. 50, pp. 705–719, Oct. 15, 1936.

[4] W. Shockley, "Electronic energy bands in sodium chloride," *Phys. Rev.*, vol. 50, pp. 754–759, Oct. 15, 1936.

[5] J. B. Fisk, L. I. Schiff, and W. Shockley, "On binding of neutrons and protons," *Phys. Rev.*, vol. 50, no. 11, pp. 1090–1091, Dec. 1, 1936.

[6] W. Shockley, "Energy bands for the face-centered lattice," *Phys. Rev.*, vol. 51, pp. 129–135, Jan. 15, 1937.

[7] ——, "The empty lattice test of the cellular methods in solids," *Phys. Rev.*, vol. 52, no. 8, pp. 866–872, Oct. 15, 1937.

[8] ——, "Theory of order for the copper gold alloy system," *J. Chem. Phys.*, vol. 6, no. 3, pp. 130–144, Mar. 1938.

[9] F. C. Nix and W. Shockley, "Order-disorder transformations in alloys," *Rev. Modern Phys.*, vol. 10, no. 1, pp. 1–71, Jan. 1938.

[10] W. Shockley and J. R. Pierce, "A theory of noise for electron multipliers," *Proc. IRE*, vol. 26, pp. 321–332, Mar. 1938.

[11] C. E. Fay, A. L. Samuel, and W. Shockley, "On the theory of space charge between parallel plane electrodes," *Bell Syst. Tech.*

J., vol. XVII, pp. 49–79, Jan. 1938.
[12] W. Shockley, "On the interaction of atoms in alloys," *J. Chem. Phys.*, vol. 6, no. 9, pp. 523–525, Sept. 1938.
[13] ——, "Currents to Conductors induced by a moving point charge," *J. Appl. Phys.*, vol. 9, no. 10, pp. 635–636, Oct. 1938.
[14] J. Steigman, W. Shockley, and F. C. Nix, "The self-diffusion of copper," *Phys. Rev.*, 2nd series, vol. 56, pp. 13–21, July 1, 1939.
[15] W. Shockley, "Nature of the metallic state," *J. Appl. Phys.*, vol. 10, no. 8, pp. 543–555, Aug. 1939.
[16] ——, "On the surface states associated with a periodic potential," *Phys. Rev.*, vol. 56, no. 4, pp. 317–323, Aug. 15, 1939.
[17] ——, "The quantum physics of solids, I—The energies of electrons in crystals," *Bell Syst. Tech. J.*, vol. XVIII, pp. 645–723, Oct. 1939.
[18] J. Bardeen, W. H. Brattain, and W. Shockley, "Investigation of oxidation of copper by use of radioactive Cu tracer," *J. Chem. Phys.*, vol. 14, no. 12, pp. 714–721, Dec. 1946.
[19] W. H. Brattain and W. Shockley, "Density of surface states on silicon deduced from contact potential measurements," *Phys. Rev.*, vol. 72, no. 4, p. 345, Aug. 15, 1947.
[20] R. D. Heidenreich and W. Shockley, "Electron microscope and electron-diffraction study of slip in metal crystals," *J. Appl. Phys.*, vol. 18, no. 11, pp. 1029–1031, Nov. 1947.
[21] ——, "Study of slip in aluminum crystals by electron microscope and electron diffraction methods," in *Proc. Conf. Strength of Solids*, H. H. Wills Physical Laboratory, Univ. Bristol, U.K., July 7–9, 1947, pp. 57–75. Reprinted in Bell Telephone System Tech. Pub., *Monograph B-1618*, pp. 1–21.
[22] J. R. Haynes and W. Shockley, "The trapping of electrons in silver chloride," in *Physical Society Bristol Conf. Rep.*, London, U.K., 1948, pp. 151–157.
[23] W. P. Mason, H. J. McSkimin, and W. Shockley, "Ultrasonic observation of twinning in tin," *Phys. Rev.*, vol. 73, no. 10, pp. 1213–1214, May 15, 1948.
[24] W. Shockley and G. L. Pearson, "Modulation of conductance of thin films of semi-conductors by surface charges," *Phys. Rev.*, vol. 74, pp. 232–233, July 15, 1948.
[25] H. J. Williams, R. M. Bozorth, and W. Shockley, "Magnetic domain patterns on single crystals of silicon iron," *Phys. Rev.*, vol. 75, no. 1, pp. 155–178, Jan. 1, 1949.
[26] H. J. Williams and W. Shockley, "A simple domain structure in an iron crystal showing a direct correlation with the magnetization," *Phys. Rev.*, vol. 75, pp. 178–183, Jan. 1, 1949.
[27] E. J. Ryder and W. Shockley, "Interpretation of dependence of resistivity of germanium on electric field," *Phys. Rev.*, vol. 75, p. 310, Jan. 15, 1949.
[28] J. R. Haynes and W. Shockley, "Investigation of hole injection in transistor action," *Phys. Rev.*, vol. 75, p. 691, Feb. 15, 1949.
[29] W. Shockley and W. T. Read, "Quantitative predictions from dislocation models of crystal grain boundaries," *Phys. Rev.*, vol. 75, no. 4, p. 692, Feb. 15, 1949.
[30] H. Suhl and W. Shockley, "Concentrating holes and electrons by magnetic fields," *Phys. Rev.*, vol. 75, no. 10, pp. 1617–1618, May 15, 1949.
[31] W. Shockley, "Dislocation theory, in cold working of metals," *Amer. Soc. Metals*, pp. 131–147, 1949.
[32] W. Shockley and J. Bardeen, "Energy bands and mobilities in monatomic semiconductors," *Phys. Rev.*, vol. 77, no. 3, pp. 407–408, Feb. 1, 1950.
[33] W. Shockley, G. L. Pearson, and J. R. Haynes, "Hole injection in germanium—Quantitative studies and filamentary transistors," *Bell Syst. Tech. J.*, vol. XXVIII, no. 3, pp. 344–366, July 1949.
[34] W. Shockley, "The theory of p-n junctions in semiconductors and p-n junction transistors," *Bell Syst. Tech. J.*, vol. XXVIII, no. 3, pp. 435–489, July 1949.
[35] C. Kittel, E. A. Nesbitt, and W. Shockley, "Theory of magnetic properties and nucleation in alnico V," *Phys. Rev.*, vol. 77, no. 6, pp. 839–840, Mar. 15, 1950.
[36] W. Shockley, "Energy band structures in semiconductors," *Phys. Rev.*, vol. 78, no. 2, pp. 173–174, Apr. 15, 1950.
[37] W. T. Read and W. Shockley, "Dislocation models of crystal grain boundaries," *Phys. Rev.*, vol. 78, no. 3, pp. 275–289, May 1, 1950.
[38] W. Shockley, "Theories of high values of alpha for collector contacts on germanium," *Phys. Rev.*, vol. 78, no. 3, pp. 294–295, May 1, 1950.
[39] G. L. Pearson, J. R. Haynes, and W. Shockley, "Comment on mobility anomalies in germanium," *Phys. Rev.*, vol. 78, no. 3, pp. 295–296, May 1, 1950.
[40] W. Shockley, "Effect of magnetic fields on conduction—Tube integrals," *Phys. Rev.*, vol. 79, no. 1, pp. 191–192, July 1, 1950.
[41] ——, "Holes and electrons," *Phys. Today*, vol. 3, no. 10, pp. 16–24, Oct. 1950.
[42] J. Bardeen and W. Shockley, "Scattering of electrons in crystals in the presence of large electric fields," *Phys. Rev.*, vol. 80, no. 1, pp. 69–71, Oct. 1, 1950.
[43] ——, "Deformation potentials and mobilities in non-polar crystals," *Phys. Rev.*, vol. 80, no. 1, pp. 72–80, Oct. 1, 1950.
[44] H. J. Williams, W. Shockley, and C. Kittel, "Studies of the propagation velocity of a ferromagnetic domain boundary," *Phys. Rev.*, vol. 80, no. 6, pp. 1090–1094, Dec. 15, 1950.
[45] E. J. Ryder and W. Shockley, "Mobilities of electrons in high electric fields," *Phys. Rev.*, vol. 81, no. 1, pp. 139–140, Jan. 1, 1951.
[46] F. S. Goucher, G. L. Pearson, M. Sparks, G. K. Teal, and W. Shockley, "Theory and experiment for a germanium p-n junction," *Phys. Rev.*, vol. 81, no. 4, pp. 637–638, Feb. 15, 1951.
[47] J. R. Haynes and W. Shockley, "The mobility and life of injected holes and electrons in germanium," *Phys. Rev.*, vol. 81, no. 5, pp. 835–843, Mar. 1, 1951.
[48] J. R. Haynes and W. Shockley, "The mobility of electrons in silver chloride," *Phys. Rev.*, vol. 82, no. 6, pp. 935–943, June 15, 1951.
[49] W. Shockley, M. Sparks, and G. K. Teal, "p-n junction transistors," *Phys. Rev.*, vol. 83, no. 1, pp. 151–162, July 1, 1951.
[50] W. Shockley, "Hot electrons in germanium and Ohm's law," *Bell Syst. Tech. J.*, vol. XXX, no. 4, part 1, pp. 990–1034, Oct. 1951.
[51] K. B. McAfee, E. J. Ryder, W. Shockley, and M. Sparks, "Observations of zenar current in germanium p-n junctions," *Phys. Rev.*, vol. 83, no. 3, pp. 650–651, Aug. 1, 1951.
[52] W. Shockley, "New phenomena of electronic conduction in semi-conductors," *Phys. Today*, pp. 26–36, 1951.
[53] G. L. Pearson, W. T. Read, and W. Shockley, "Probing the space-charge layer in a p-n junction," *Phys. Rev.*, vol. 85, no. 6, pp. 1055–1057, 15th Mar. 1952.
[54] K. B. McAfee, W. Shockley, and M. Sparks, "Measurement of diffusion in semiconductors by a capacitance method," *Phys. Rev.*, vol. 86, no. 1, pp. 137–138, Apr. 1, 1952.
[55] W. T. Read, Jr., and W. Shockley, "On the geometry of dislocations," in *Imperfections in Nearly Perfect Crystals*. New York: Wiley, 1952, ch. 2, pp. 77–94.
[56] ——, "Dislocation models of grain boundaries," in *Imperfections in Nearly Perfect Crystals*. New York: Wiley, 1952, ch. 13, pp. 352–376.
[57] W. Shockley, "Solid state physics in electronics and in metallurgy," *Trans. AIME, J. Metals*, vol. 194, pp. 829–842, Aug. 1952.
[58] W. Shockley and W. T. Read, Jr., "Statistics of the recombinations of holes and electrons," *Phys. Rev.*, vol. 87, no. 5, pp. 935–842, Sept. 1, 1952.
[59] W. Shockley, "Interpretation of e/m values for electrons in crystals," *Phys. Rev.*, vol. 88, no. 4, p. 953, Nov. 15, 1952.
[60] ——, "Transistor electronics: Imperfections, unipolar and analog transistors, *Proc. IRE*, vol. 40, pp. 1289–1313, Nov. 1952.
[61] ——, "A unipolar 'field-effect' transistor," *Proc. IRE*, vol. 40, pp. 1365–1376, Nov. 1952.
[62] T. S. Benedict and W. Shockley, "Microwave observation of the collision frequency of electrons in germanium," *Phys. Rev.*, vol. 89, no. 5, pp. 1152–1153, Mar. 1, 1953.
[63] J. D. Eshelby, W. T. Read, and W. Shockley, "Anisotropic elasticity with applications to dislocation theory," *Acta Metallurgica*, vol. 1, pp. 251–259, May 1953.
[64] W. Shockley, "Cyclotron resonances, magnetoresistance, and Brillouin Jones in semiconductors," *Phys. Rev.*, vol. 90, no. 3, p. 491, May 1, 1953.
[65] W. Shockley and R. C. Prim, "Space-charge limited emission in semiconductors," *Phys. Rev.*, vol. 90, no. 5, pp. 753–758, June 1, 1953.
[66] W. Shockley, "Some predicted effects of temperature gradients on diffusion in crystals," *Phys. Rev.*, vol. 91, no. 6, pp. 1563–1564, Sept. 15, 1953.
[67] J. R. Tesman, A. H. Kahn, and W. Shockley, "Electronic polarizabilities of ions in crystals," *Phys. Rev.*, vol. 92, no. 4,

pp. 890–895, Nov. 15, 1953.
[68] R. C. Prim and W. Shockley, "Joining solutions at the pinch-off in 'field-effect' transistor," *Trans. IRE, Professional Group Electron Devices*, vol. PGED-4, pp. 1–14, Dec. 1953.
[69] W. Shockley, "Transistor physics," *Amer. Scientist*, vol. 42, no. 1, pp. 41–72, Jan. 1954.
[70] ——, "Some predicted effects of temperature gradients on diffusion in crystals," *Phys. Rev.*, vol. 93, no. 2, pp. 345–346, Jan. 15, 1954.
[71] W. Shockley and W. P. Mason, "Dissected amplifiers using negative resistance," *J. Appl. Phys.*, vol. 25, no. 5, p. 677, May 1954.
[72] W. van Roosebroeck and W. Shockley, "Photon-radiative recombination of electrons and holes in germanium," *Phys. Rev.*, vol. 94, no. 6, pp. 1558–1560, June 15, 1954.
[73] W. Shockley, "Negative resistance arising from transit time in semiconductor diodes," *Bell Syst. Tech. J.*, vol. XXXIII, no. 4, pp. 799–826, July 1954.
[74] ——, "Les semi-conducteurs," *Le Vide*, no. 56, pp. 9–26, Mar./Avr. 1955 (French adaptation of three conferences presented in English at the Sorbonne, Oct. 1953).
[75] ——, "Transistor physics," *Proc. Inst. Elect. Eng.*, vol. 103, pt. B, no. 7, pp. 23–41, Jan. 1956.
[76] ——, "Localized radiation damage as a means of studying vacancies and interstitials," in *Dislocations and Mechanical Properties of Crystals*, J. C. Fisher, W. G. Johnston, R. Thomson, and T. Vreeland, Jr., Eds. New York: Wiley, 1957, pp. 581–586.
[77] ——, "Transistor technology evokes new physics," *Les Prix Nobel, en 1956*, Nobel lecture, Stockholm, Sweden, pp. 100–129, Dec. 11, 1956.
[78] ——, "On the statistics of individual variations of productivity in research laboratories," *Proc. IRE*, vol. 45, pp. 279–290, Mar. 1957.
[79] B. F. Miesner and W. Shockley, "On the statistics of individual variations of productivity in research laboratories," *Proc. IRE*, vol. 45, pp. 1409–1410, Oct. 1957.
[80] P. D. Allison, J. A. Stewart, and W. Shockley, "Productivity differences among scientists: evidence for accumulative advantage," *Amer. Soc. Rev.*, vol. 39, pp. 596–606, Aug. 1974.
[81] W. Shockley and J. T. Last, "Statistics of the charge distribution for a localized flaw in a semiconductor," *Phys. Rev.*, vol. 107, no. 2, pp. 392–396, July 15, 1957.
[82] W. Shockley, "The statistics of quality losses in civil service laboratories," National Academy of Sciences, National Research Council, NAS-ARDC Special Study COM-4-T19, pp. 1–14, Oct. 1957.
[83] ——, "Unique properties of the four-layer diode," *Electron. Ind. Tele Tech*, Aug. 1957.
[84] C.-T. Sah, R. N. Noyce, and W. Shockley, "Carrier generation and recombination in P-N junctions and P-N junction characteristics," *Proc. IRE*, vol. 45, pp. 1228–1243, Sept. 1957.
[85] W. Shockley and J. F. Gibbons, "Introduction to the four-layer diode," *Semiconductor Products*, vol. 1, no. 1, pp. 9–13, Jan./Feb. 1958.
[86] W. Shockley, "Guest editorial," *Semiconductor Products*, p. 5, Mar./Apr. 1958.
[87] C.-T. Sah and W. Shockley, "Electron-hole recombination statistics in semiconductors through flaws with many charge conditions," *Phys. Rev.*, vol. 109, no. 4, pp. 1103–1115, Feb. 15, 1958.
[88] W. Shockley, "Transistor electronics has good future," *Ind. Laboratories*, pp. 52–53, May 1958.
[89] ——, "Electron, holes and traps," *Proc. IRE*, vol. 46, pp. 973–990, June 1958.
[90] ——, "An invited essay on transistor business," *Proc. IRE*, vol. 46, pp. 954–955, June 1958.
[91] ——, "Predicted intervalley scattering effects in germanium," *Phys. Rev.*, vol. 110, no. 5, pp. 1207–1208, June 1, 1958.
[92] W. Shockley and J. F. Gibbons, "Study of ultimate high frequency and high power limits of semiconductor devices," U.S. Army Signal Corps Engineering Laboratories, Fort Monmouth, NJ, Final Rep., July 1, 1957–Oct. 15, 1958.
[93] W. Shockley and J. F. Gibbons, "Theory of transient build-up in avalanche transistor," *Commun. Electron.*, vol. 40, p. 993, Jan. 1959. Reprinted from *Solid State Physics in Electronics and Telecommunications*. London, U.K.: Academic, 1958, pp. 1024–1035.
[94] W. Shockley and J. F. Gibbons, "Current build-up in semiconductor devices," *Proc. IRE*, vol. 46, pp. 1947–1949, Dec. 1958.
[95] D. J. Hamilton, J. F. Gibbons, and W. Shockley, "Physical principles of avalanche transistor pulse circuits," *Proc. IRE*, vol. 47, pp. 1102–1108, June 1959.
[96] A. Goetzberger and W. Shockley, "Localized excess reverse currents in silicon p-n junctions," in *Structure and Properties of Thin Films*. New York: Wiley, 1959, pp. 298–301.
[97] K. Hubner and W. Shockley, "Analysis of diffusion down dislocations," in *Structure and Properties of Thin Films*. New York: Wiley, 1959, pp. 302–305.
[98] W. Shockley, "Theory of transmitted phonon drag," in *Structure and Properties of Thin Films*. New York: Wiley, 1959, pp. 306–327.
[99] ——, "The four-layer transistor diode: An example of a solid state circuit or molecular engineering," *Wave Guide*, vol. X, no. 7, Mar. 1959.
[100] ——, "Transistor-diodes," *Proc. Inst. Elect. Eng.*, vol. 106, pt. B, suppl. 15, pp. 270–272, May 21, 1959.
[101] ——, "Discussion on basic theory-II (minimum capacity junction)," *Proc. Inst. Elect. Eng.*, vol. 106, pt. B, suppl. 17, May 22, 1959.
[102] K. Hubner and W. Shockley, "Transmitted phonon drag measurements in silicon," *Phys. Rev. Lett.*, vol. 4, no. 10, pp. 504–505, May 15, 1960.
[103] ——, "Transmitted phonon drag measurements in silicon," in *Proc. Int. Conf. Semiconductor Physics*, Prague, Czechoslovakia, 1960, pp. 229–231.
[104] W. Shockley and J. L. Moll, "Solubility of flaws in heavily-doped semiconductors," *Phys. Rev.*, vol. 119, no. 5, pp. 1480–1482, Sept. 1, 1960.
[105] A. Goetzberger and W. Shockley, "Metal precipitates in silicon p-n junctions," *J. Appl. Phys.*, vol. 31, no. 10, pp. 1821–1824, Oct. 1960.
[106] W. Shockley, "Problems related to p-n junctions in silicon," *Solid State Electron.*, vol. 2, no. 1, pp. 35–67, Jan. 1961.
[107] K. Hubner and W. Shockley, "New experiments on interaction of phonons with crystalline defects," in *Advanced Energy Conversion*. London, U.K.: Pergamon, 1961, vol. 1, pp. 93–96.
[108] M. A. Melehy and W. Shockley, "Response of a p-n junction to a linearly decreasing current," *Trans. IRE, Professional Group Electron Devices*, vol. PGED-8, no. 2, pp. 135–139, Mar. 1961.
[109] W. Shockley and H. J. Queisser, "Detailed balance limit of efficiency of p-n junction solar cells," *J. Appl. Phys.*, vol. 32, pp. 510–519, Mar. 1961. Reprinted in *Solar Cells*, C. E. Backus, Ed. New York: IEEE Press, 1976, pp. 136–145.
[110] H. J. Queisser and W. Shockley, "Some theoretical aspects of the physics of solar cells," in *Progress in Astronautics and Rocketry*, vol. 3, *Energy Conversion for Space Power*. New York: Academic, 1961, pp. 317–323.
[111] H. J. Queisser, K. Hubner, and W. Shockley, "Diffusion along small-angle grain boundaries in silicon," *Phys. Rev.*, vol. 123, no. 4, pp. 1245–1254, Aug. 15, 1951.
[112] W. Shockley, "Field enhanced donor diffusion in degenerate semiconductor layers," *J. Appl. Phys.*, vol. 32, p. 1402, July 1961.
[113] ——, "Diffusion and drift of minority carriers in semiconductors for comparable capture and scattering mean free paths," *Phys. Rev.*, vol. 125, no. 5, pp. 1570–1576, Mar. 1, 1962.
[114] W. Shockley and A. Goetzberger, "The role of imperfections in semiconductor devices," *Proc. AIME*, pp. 121–135, 1962.
[115] K. Hubner and W. Shockley, "Measurement of phonon scattering by a small angle grain boundary in silicon," presented at the International Conference on Physics of Semiconductors, Institute of Physics and the Physical Society, Exeter, U.K., July 1962.
[116] H. J. Queisser and W. Shockley, "Diffusion-induced slip in silicon and the problem of dislocation distribution," in *Proc. 1st Berkeley Int. Materials Conf.*, Univ. California, Berkeley, 1963, pp. 781–789.
[117] R. M. Scarlett, W. Shockley, and R. H. Haitz, "Thermal instabilities and hot spots in junction transistors," *Physics of Failure in Electronics*, M. F. Goldberg, Ed. Baltimore, MD: Cleaver-Hume, 1963, pp. 194–203.
[118] R. M. Scarlett and W. Shockley, "Secondary breakdown and hot spots in power transistors," in *IEEE Int. Convention Rec.*, 1963, pt. 3, pp. 3–13.

[119] W. Shockley, "Engineering challenges and human welfare," *Engineer's Week*, 1963.
[120] W. Shockley, D. R. Curran, and D. J. Koneval, "Energy trapping and related studies of multiple electrode filter crystals," in *Proc. 17th Ann. Symp. Frequency Control*, U.S. Army Electronics Research and Development Laboratory, Fort Monmouth, NJ, May 27–29, 1963, pp. 88–126.
[121] R. H. Haitz, A. Goetzberger, R. M. Scarlett, and W. Shockley, "Avalanche effects in silicon p-n junctions, I: Localized photomultiplication studies on microplasmas," *J. Appl. Phys.*, vol. 34, no. 6, pp. 1581–1590, June 1963.
[122] W. Shockley, "Scientific thinking and problems of growth," *Impact of Science: California and the Challenge of Growth, University of California*. San Diego, CA: Univ. California Printing Department, 1963, pp. 90–103.
[123] ——, "Transistor history, applied research and science teaching," invited lecture, in *Proc. 75th Anniversary Meeting Japanese Institution of Electrical Engineers*, vol. 84-2, no. 905, 1963, pp. 147–158.
[124] W. Shockley, H. J. Queisser, and W. W. Hooper, "Charges on oxidized silicon surfaces," *Phys. Rev. Lett.*, vol. 11, no. 11, pp. 489–490, Dec. 1, 1963.
[125] W. Shockley and F. J. McDonald, "Teaching scientific thinking at the high school level," Final Rep., Project S-090, U.S. Dept. Health, Education and Welfare, Office of Education Contract OE 4-10-216, School of Engineering and School of Education, Stanford Univ., Stanford, CA, 1964.
[126] M. G. Buehler, W. Shockley, and G. L. Pearson, "Hall measurements using Corbino-like current sources in thin circular disks," *Appl. Phys. Lett.*, vol. 5, no. 11, pp. 228–229, Dec. 1, 1964.
[127] W. Shockley and W. W. Hooper, "The surface controlled avalanche transistor," in *Proc. Frontiers in Electronics Western Electronic Show and Convention*, Los Angeles, CA, Aug. 25–28, 1964, pp. 1–3; see also *Electronic Products*, vol. 7, p. 68, 1964.
[128] W. Shockley, W. W. Hooper, H. J. Queisser, and W. Schroen, "Mobile electric charges on insulating oxides with application to oxide covered silicon p-n junctions," in *Surface Science*. Amsterdam, The Netherlands: North-Holland, 1964, vol. 2, pp. 277–287.
[129] W. Shockley, lecture notes on "Respect for the scientific nature of practical problems, and recognize the inadequacies in the 'law of excluded optimum,' as far as government agencies are concerned," in *Proc. 3rd Navy Microelectronics Program Conf.* Apr. 5, 1965. (Lecture notes taken and reconstructed by G. S. Szekely.)
[130] R. Gereth and W. Shockley, "Study of radiation damage by using field effect," *Proc. IEEE*, vol. 53, pp. 748–749, July 1965.
[131] W. Shockley, J. A. Copeland, and R. P. James, "The impedance field method of noise calculation in active semiconductor devices," in *Quantum Theory of Atoms, Molecules, Solid State*. New York: Academic, pp. 537–563.
[132] W. Shockley, "Articulated science teaching and balanced emphasis," *IEEE Spectrum*, vol. 3, no. 6, pp. 49–58, June 1966. Reprinted in *Communication Concepts and Perspectives*. Washington, DC: Spartan, 1967, pp. 153–179.
[133] J. W. Allen, W. Shockley, and G. L. Pearson, "Gunn domain dynamics," *J. Appl. Phys.*, vol. 37, no. 8, pp. 3191–3195, July 1966.
[134] Y. S. Chen, W. Shockley, and G. L. Pearson, "Lattice vibration spectra of $GaAs_xP_{1-x}$ single crystals," *Phys. Rev.*, vol. 151, no. 2, pp. 648–656, Nov. 11, 1966.
[135] W. Shockley, "Articulated science teaching and balanced emphasis," 37th Memorial Steinmetz Lecture, *IEEE Spectrum*, vol. 3, no. 6, pp. 49–58, 1966.
[136] W. Shockley and R. P. James, "A 'try simplest cases' development of forces on magnetic current," Bell Telephone Laboratories Technical Memo. with Abstract, Manuscript, and Diagrams, MM 67-25-1, Mar. 27, 1967.
[137] W. Shockley, D. R. Curran, and D. J. Koneval, "Trapped-energy modes in quartz filter crystals," *J. Acoust. Soc. Amer.*, vol. 41, no. 4 (pt. 2), pp. 981–993, Apr. 1967.
[138] W. Shockley and R. P. James, "'Try simplest cases' discovery of 'hidden momentum' forces on 'magnetic currents,'" *Phys. Rev. Lett.*, vol. 18, no. 20, CY501 (C), CY501 1-4, 2-4, 3-4, 4-4, pp. 876–879, May 15, 1965.
[139] W. Shockley, responses to " 'Try simplest cases' discovery of 'hidden momentum' forces on 'magnetic currents,' " *Ind. Res.*, p. 16, June 1967; *Bell Laboratories Rec.*, p. 99, Mar. 1968; and *SCOPE—Stanford Electronics Laboratories*, vol. V, no. 2, Fall 1968.
[140] S. M. Sze and W. Shockley, "Unit-cube expression for space-charge resistance," *Bell Syst. Tech. J.*, vol. XLVI, no. 5, pp. 837–842, May–June 1967.
[141] W. Shockley, "Hidden linear momentum" related to the E-term for a Dirac-electron wave packet in an electrical field," *Phys. Rev. Lett.*, vol. 20, no. 7, p. 343 (C)-346, Feb. 12, 1968.
[142] W. Shockley, P. D. Hurd, and F. J. McDonald, "The conservation of energy concept in ninth grade general science," U.S. Department of Health, Education and Welfare, Office of Education, Bureau of Research, Final Rep., Project no. OE 6-10-026, Feb. 1968, pp. i–ix, 1–84.
[143] W. Shockley, "A 'try simplest cases' resolution of the Abraham–Minkowski controversy on electromagnetic momentum in matter," *Proc. Nat. Acad. Sci.*, vol. 60, no. 3, pp. 807–813, July 1968.
[144] W. Shockley and K. K. Thornber, "The 'hidden momentum' equivalent to magnetic charges for a bound-state Dirac electron," *Phys. Lett.*, vol. 27A, no. 8, pp. 534–535, Sept. 9, 1968.
[145] W. Shockley, "Thinking about thinking improves thinking," *IEEE Student J.*, pp. 11–16, Sept. 1968.
[146] A. J. Kurtzig and W. Shockley, "A new direct measurement of the domain wall energy of the orthoferrites," *IEEE Trans. Magn.*, vol. MAG-4, pp. 426–430, Sept. 1968.
[147] A. J. Kurtzig and W. Shockley, "Measurement of the domain-wall energy of the orthoferrites," *J. Appl. Phys.*, vol. 39, no. 12, pp. 5619–5630, Nov. 1968.
[148] W. Shockley, "S-ambiguity of Poynting's integral theorem eliminated by conceptual experiments with pulsed current distributions," *Phys. Lett.*, vol. 28A, no. 3, pp. 185–186, Nov. 18, 1968.
[149] W. Shockley and K. K. Thornber, "Hidden momentum for non-steady-state defined using a new mass-moment operator theorem for Dirac's equation," *Phys. Lett.*, vol. 34A, no. 3, pp. 177–178, Feb. 22, 1971.
[150] W. Shockley, "Stark ladders for finite one-dimensional models of crystals," *Phys. Rev. Lett.*, vol. 28, no. 6, pp. 349–352, Feb. 7, 1972.
[151] ——, "Three men who changed our world—25 years later," *Bell Telephone Laboratories Rec.*, Dec. 1972.
[152] ——, "The junction transistor," *New Scientist*, pp. 689–691, Dec. 21, 1972. Reprinted from *Bell Telephone Laboratories Rec.*, pp. 379–381, Aug. 1951.
[153] ——, "The invention of the transistor: An example of creative-failure methodology," *Solid State Devices*, pp. 55–75, 1972.
[154] ——, "The invention of the transistor—An example of creative failure methodology," National Bureau of Standards Special Publication 388, in *Proc. Conf. Public Need and the Role of the Inventor*, Monterey, CA, June 11–14, 1973, pp. 47–89.
[155] ——, "The path to the conception of the junction transistor," *IEEE Trans. Electron Devices*, vol. ED-23, pp. 597–620, July 1976. Reprinted in *IEEE Trans. Electron Devices*, vol. ED-31, pp. 1523–1545, Nov. 1984.
[156] W. Shockley, "Do dislocations hold technological promise?" *Solid State Technol.*, vol. 26, no. 1, pp. 75–78, Jan. 1983.

APPENDIX 3
SHOCKLEY BOOKS

[1] W. Shockley, *Electrons and Holes in Semiconductors with Applications in Transistor Electronics*. New York: Van Nostrand, Bell Laboratories Series, 1950.
[2] W. Shockley and W. A. Gong, *Mechanics*. Columbus, OH: C. E. Merrill Books, 1966.

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five pages from Shockley's Bell Telephone Laboratories Notebook no. 20 455 from the AT&T archives. He also is grateful to the Stanford University Cecil H. Green Library, Special Collections Department, and the archivist, M. Kimball, for free access to Shockley's papers.

REFERENCES

[1] W. B. Shockley, Bell Telephone Laboratories Notebook no. 20 455, AT&T Archives, NJ, Feb. 24, 1945–Nov. 5, 1948, pp. 128–132.
[2] M. Tanenbaum and D. E. Thomas, "Diffused emitter and base silicon transistors," *Bell Syst. Tech. J.*, vol. 35, pp. 1–22, Jan. 1956.
[3] *Grolier Encyclopedia of Knowledge*, s.v. "Famine."
[4] W. S. Churchill, *The Second World War*, vols. 1–6. Boston, MA: Houghton Mifflin, 1950.
[5] W. B. Shockley, "Population control or eugenics," in J. D. Roslansky, Ed., *Genetics and the Future of Man*. Amsterdam, The Netherlands: North-Holland, 1966.
[6] J. Bardeen and W. H. Brattain, "Three-electrode circuit element utilizing semiconductor materials," U.S. Patent 2 524 035, Oct. 3, 1950.
[7] J. A. Hoerni, personal communication, Feb. 27, 1996.
[8] ____, personal communication, Mar. 6, 1996
[9] D. C. Hoefler, "Silicon Valley, U.S.A.," *Electronic News*, pt. I, Jan. 11, 1971, pp. 1–5; pt. II, Jan. 18, 1971, pp. 1–5; pt. III, Jan. 25, 1971, pp. 4–5.
[10] J. S. Kilby, "Miniaturized electronic circuits," U. S. Patent 3 138 743, June 23, 1964.
[11] R. N. Noyce, "Semiconductor device-and-lead structure," U.S. Patent 2 981 877, Apr. 25, 1961
[12] G. E. Moore, personal communication, Aug. 7, 1996.

Probir K. Bondyopadhyay (Senior Member, IEEE), for a photograph and biography, see this issue, p. 5.