**Cost, Performance and Power Implications of Monolithic 3D Integrated Circuits**

Interconnect issues significantly impact the performance, power, and density of today’s integrated circuits. 3D technology, with shorter interconnects, offers a path to tackle these issues. The industry is pursuing 3D Through-Silicon Via (TSV) technology, which is projected by the Intl. Technology Roadmap for Semiconductors [1] to offer minimum via sizes of ~1um between 2009 and the current roadmap end (2015). While these TSV sizes can address chip-to-chip interconnect issues, on-chip interconnect difficulties can be tackled more effectively when through-silicon connections have sizes comparable to on-chip interconnect dimensions, i.e. <50nm. Monolithic 3D technology can address this need.

Two novel yet practical techniques to obtain Monolithic 3D-ICs [2] will be briefly described in this paper. The first technique constructs transistors above copper interconnect at less than 400oC. Recessed channel transistors are used for this technique. This transistor family is extensively used in DRAM manufacturing today, making adoption easier. The second technique utilizes any state-of-the-art replacement gate transistor, along with repeating layouts and a novel alignment scheme, to obtain a high density of through-silicon connections. The advantage of this technique is its compatibility with existing transistor technologies.

The bulk of the paper will describe cost, performance, and power implications of Monolithic 3D Integrated Circuits. Monolithic 3D-ICs were analyzed with a 3D version of CAD tool IntSim [3]. The study considered a 600MHz 1.6W low-power logic core constructed at the 22nm node. Results indicate that a monolithic 3D-IC with 2 device layers can provide a 2x reduction in power, a 2x reduction in total silicon area, and a 4x reduction in chip footprint (compared to a 2D-IC implementation). These benefits are mainly due to shorter interconnects with 3D, which in turn allows smaller size driver transistors, and produces die area and power reductions.

Thus, a 2-layer monolithic 3D-IC provides benefits similar to a generation of conventional scaling. Furthermore, just as Dennard scaling reduced feature sizes every generation, monolithic 3D opens the road for many years of continuous scaling by ‘folding’ once, twice, and so forth *without necessarily reducing feature sizes*.

Cost calculations using a Sematech Cost-of-Ownership framework reveal that scaling ‘up’ by doubling the number of monolithic 3D stacked device layers provides a similar cost per die benefit for logic cores as that obtained with conventional scaling. However, the existing fab upgrade capital expenditure for monolithic 3D is less than $200M, compared to the several billion dollars required for conventional scaling. This allows a broad base of semiconductor companies and older wafer fabs to participate in creating future generations of portable devices such as smart-phones and tablet computers.

References:

[1] http://public.itrs.net

[2] Z. Or-Bach, D. C. Sekar, B. Cronquist, I. Beinglass, J. L. de Jong, US Patent Application 12/847,911

[3] D. C. Sekar, J. D. Meindl, et al., “IntSim: A CAD tool for optimization of multilevel interconnect networks”, Proc. ICCAD 2007.