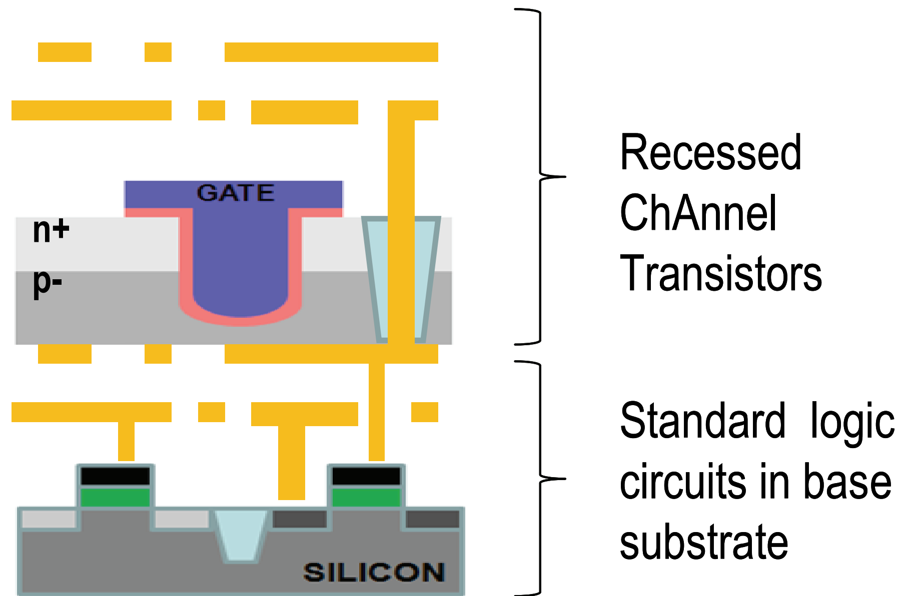
MonolithIC 3D™

Technology Breakthrough

Monolithic 3D RCAT



Technology:

The monolithic 3D IC technology is applied to producing monolithically stacked low leakage Recessed ChAnnel Transistors (RCATs), commonly used in DRAM chips since the 90nm node.

Experimental data from DRAM manufacturers indicates that RCATs can have similar drive currents and significantly lower leakage when compared to planar transistors, at the cost of higher gate capacitance.

Monolithic 3D IC provides a path to reduce logic, SOC, and memory costs without investing in expensive scaling down.

See reverse side for more on details monolithic 3D IC technology & RCAT flow

Benefits:

- 2x lower power
- 2x smaller silicon area
- 4x smaller footprint
- Layer to layer interconnect at close to full lithographic resolution and alignment
- Performance of single crystal silicon transistors on all layers in the 3DIC
- Scalable: scales normally with equipment capability
- Forestalls next gen litho-tool risk
- Also useful as AF FPGA programming transistors: programmable interconnect is 10x-50x smaller & lower power than SRAM FPGA

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www.monolithic3d.com. •Patents pending

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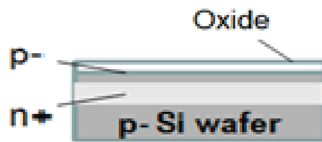
Technology Breakthrough

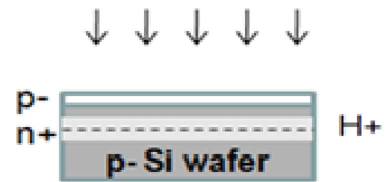
Create a layer of Recessed ChAnnel Transistors (RCATs), commonly used in DRAMs, by activating dopants at ~1000°C **before** wafer bonding to the CMOS substrate and cleaving, thereby leaving a very thin dopant stack layer from which transistors are completed, utilizing less than 400°C etch and deposition processes.

(a) Build transistors and interconnects for bottom wafer of 3D stack

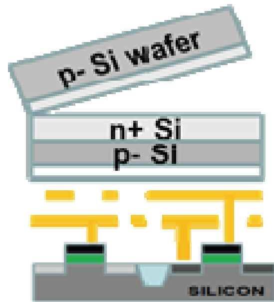
(b) Using new wafer, construct dopant regions and activate at ~1000°C



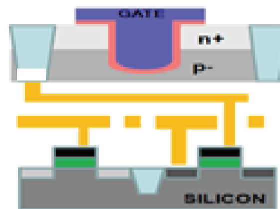
(c) Implant Hydrogen for Ion-Cut



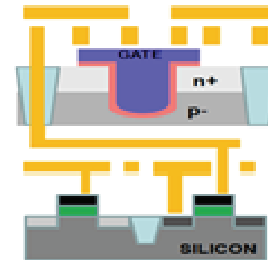
(d) Bond and Cleave, Polish



(e) Form RCATs using low temperature steps such as etch and deposition



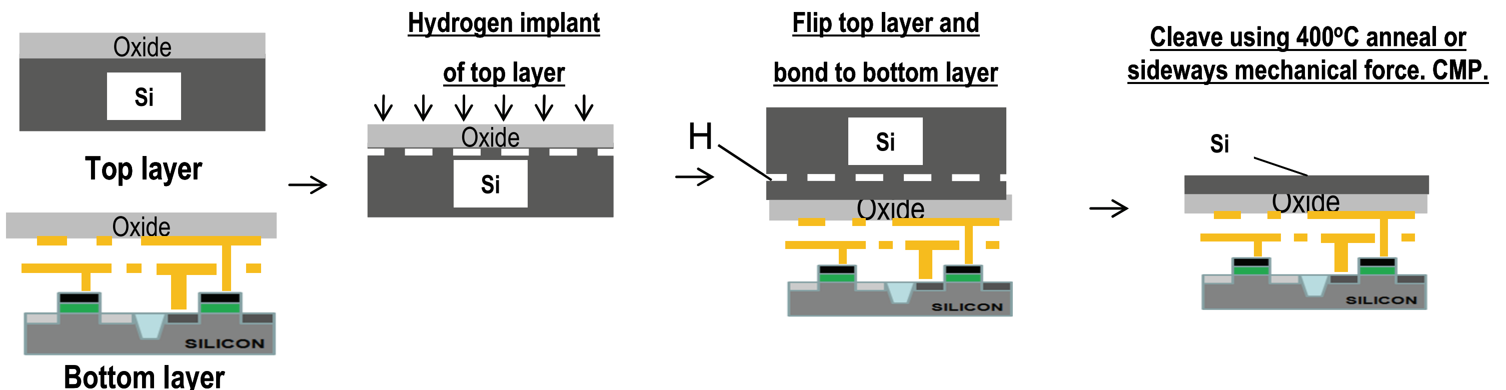
(f) Thin Silicon layer enables well-aligned top layer features



Layer Transfer Technology ("Ion-Cut")Defect-free single crystal obtained @ <400°C

Leveraging a mature technology (wafer bonding and ion-cleaving) that has been the dominant SOI wafer production method for over two decades.

Innovate and create multiple thin (10s – 100s nanometer scale) layers of virtually defect free Silicon by utilizing low temperature (<400°C) bond and cleave techniques, and place on top of active transistor circuitry. Benefit from a rich layer-to-layer interconnection density.



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