3D FPGA – The Path to ASIC-like Density, Power, and Performance

Zvi Or-Bach, NuPGA President and CEO

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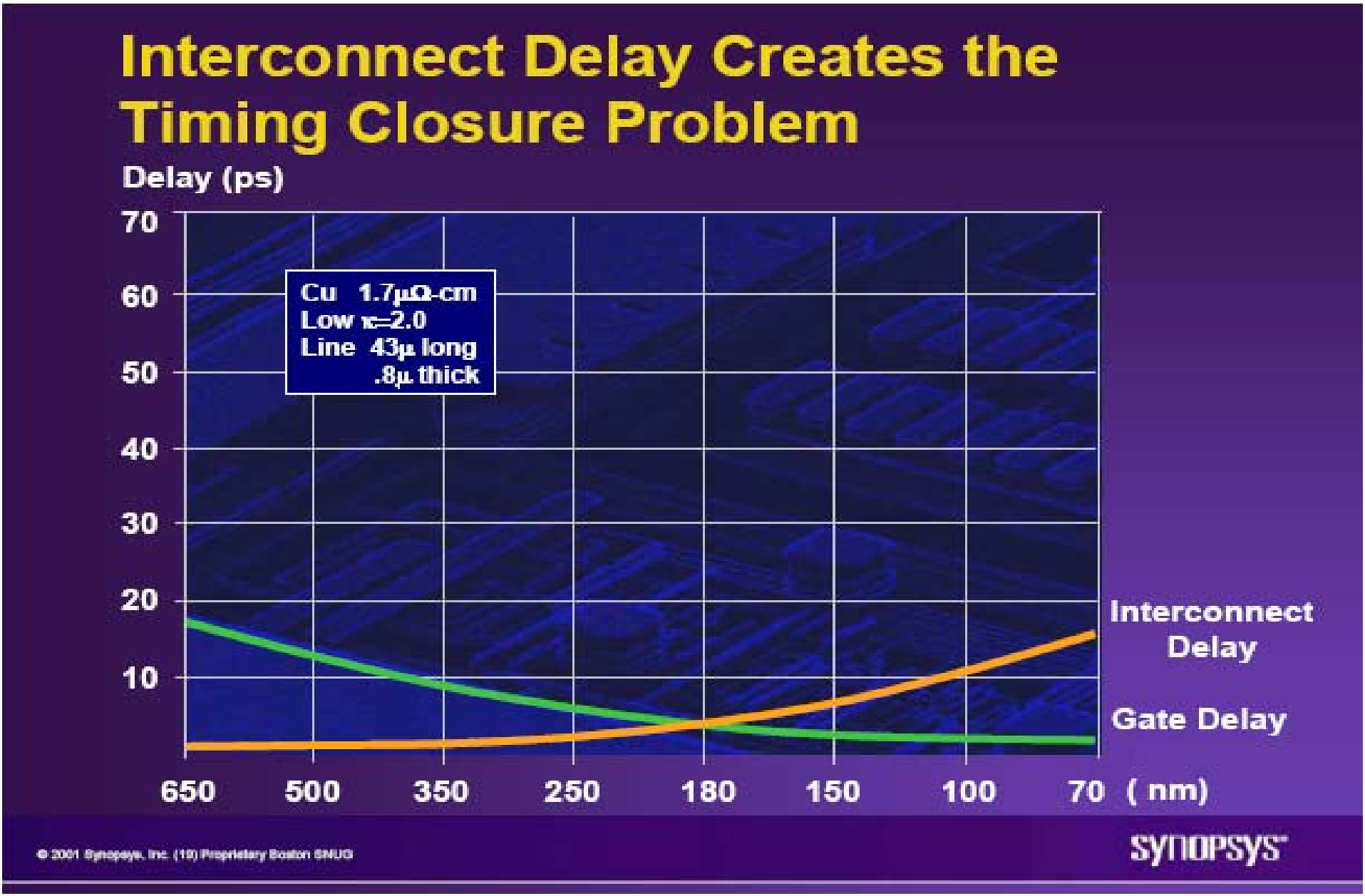
Agenda

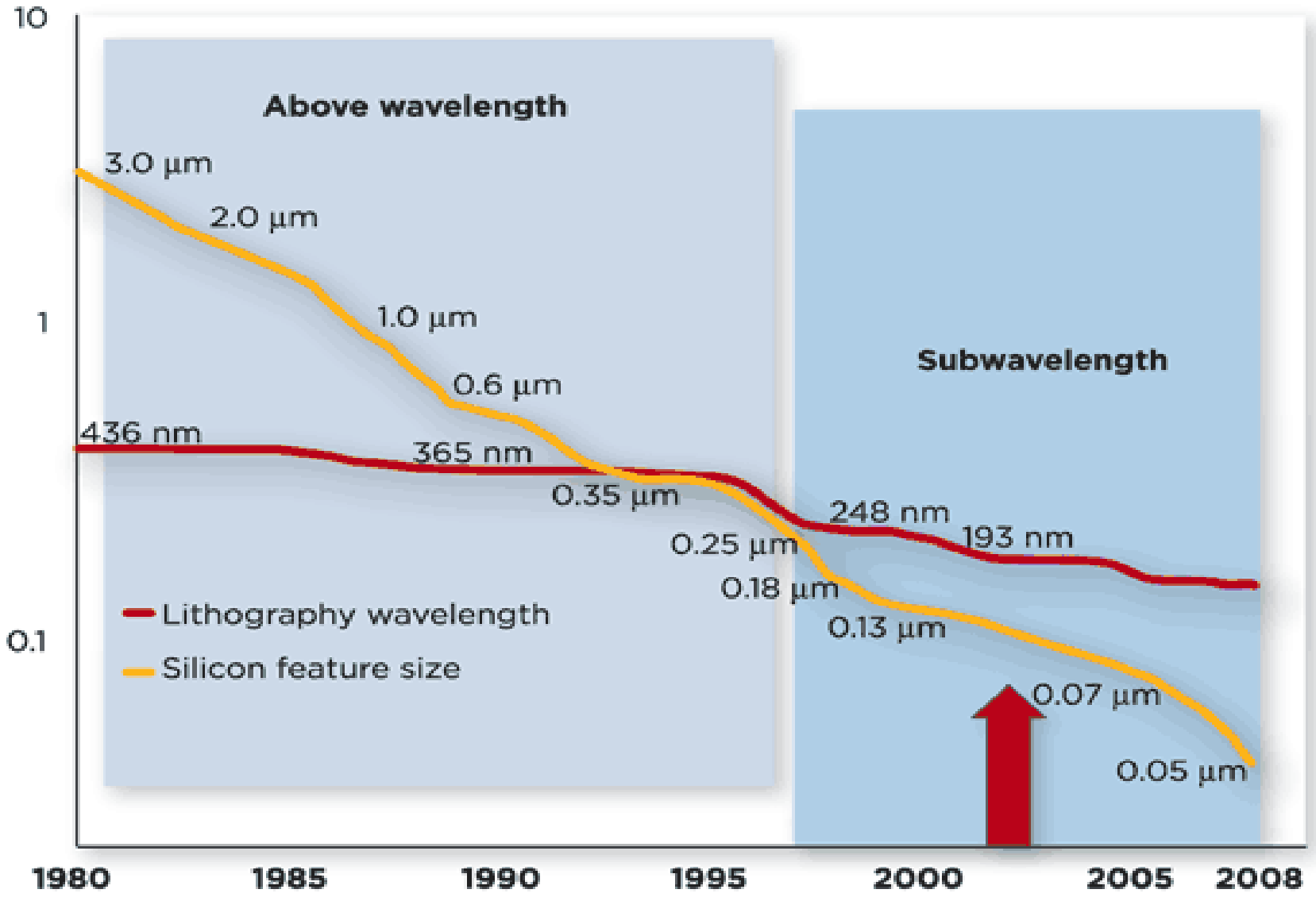
- The Logic Challenge
- Current FPGAs
- The Third Dimension
- Extension to other 3D applications
- Summary

Transistors no Longer Dominate – Metal Interconnections Took Over



As feature sizes shrink, chipmaking woes grow

Optical litho can exist only with CAD-based correction tools



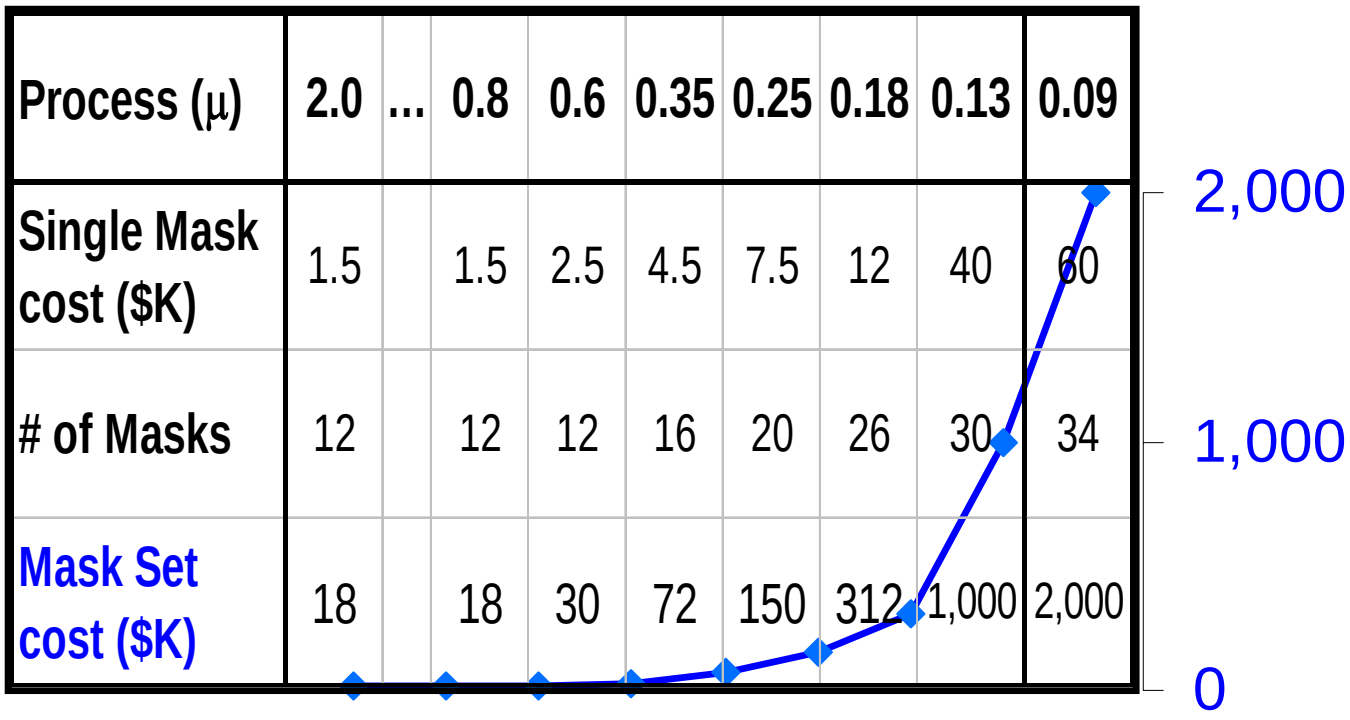
Note: vertical scale is in microns.

Source: Mentor Graphics Corp.

Accelerating Mask-Set Cost !!!

- Relative Increase of interconnection delay => More Metal Layers
- Increase in mask complexity => Mask cost increases

Process (μ)	2.0	…	0.8	0.6	0.35	0.25	0.18	0.13	0.09
Single Mask cost ($K)	1.5		1.5	2.5	4.5	7.5	12	40	60
# of Masks	12		12	12	16	20	26	30	34
Mask Set cost ($K)	18		18	30	72	150	312	1,000	2,000



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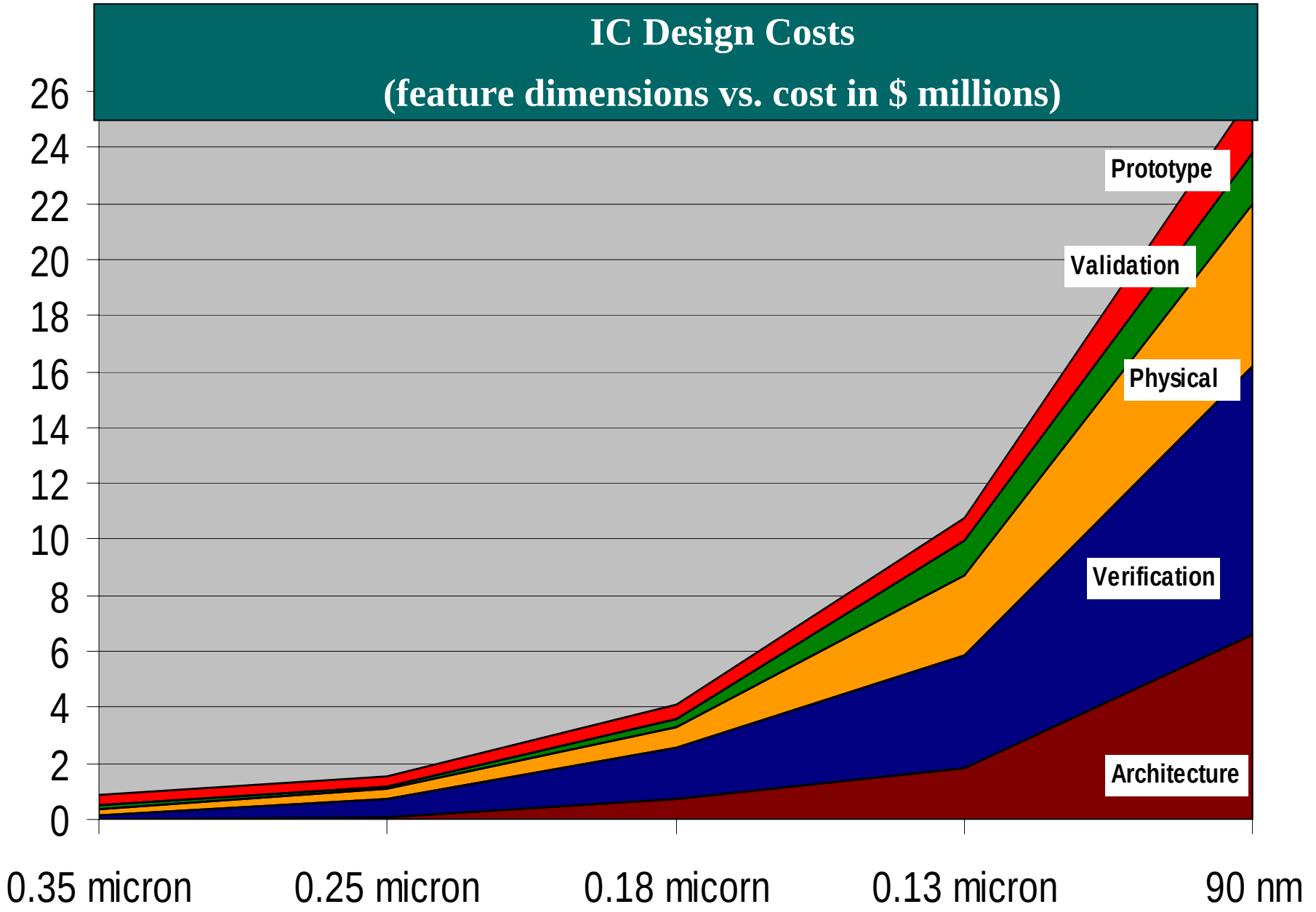
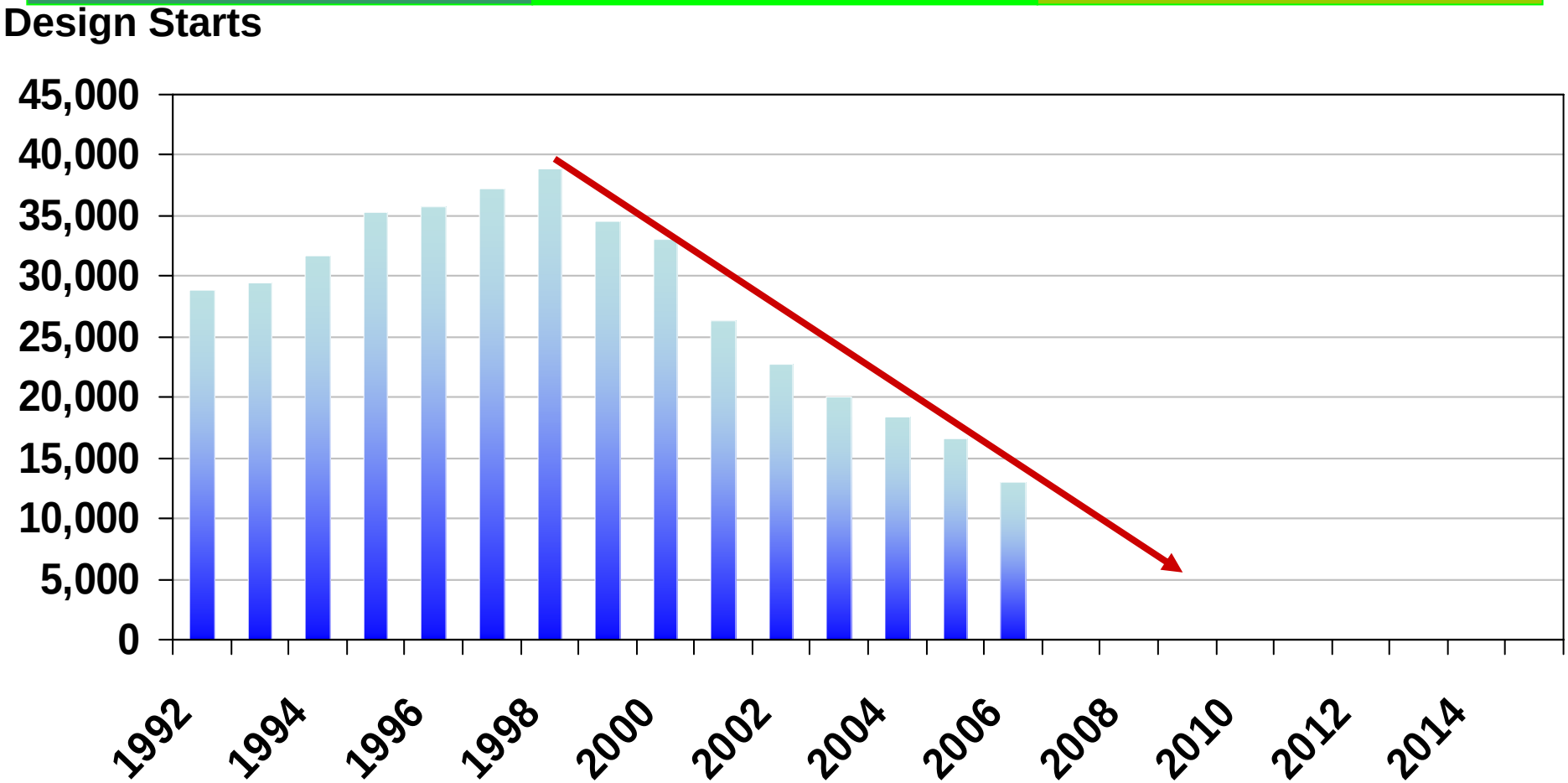


Source: International Business Strategies

Number of IC Design Starts is Collapsing



Source: VLSI Research, Inc.

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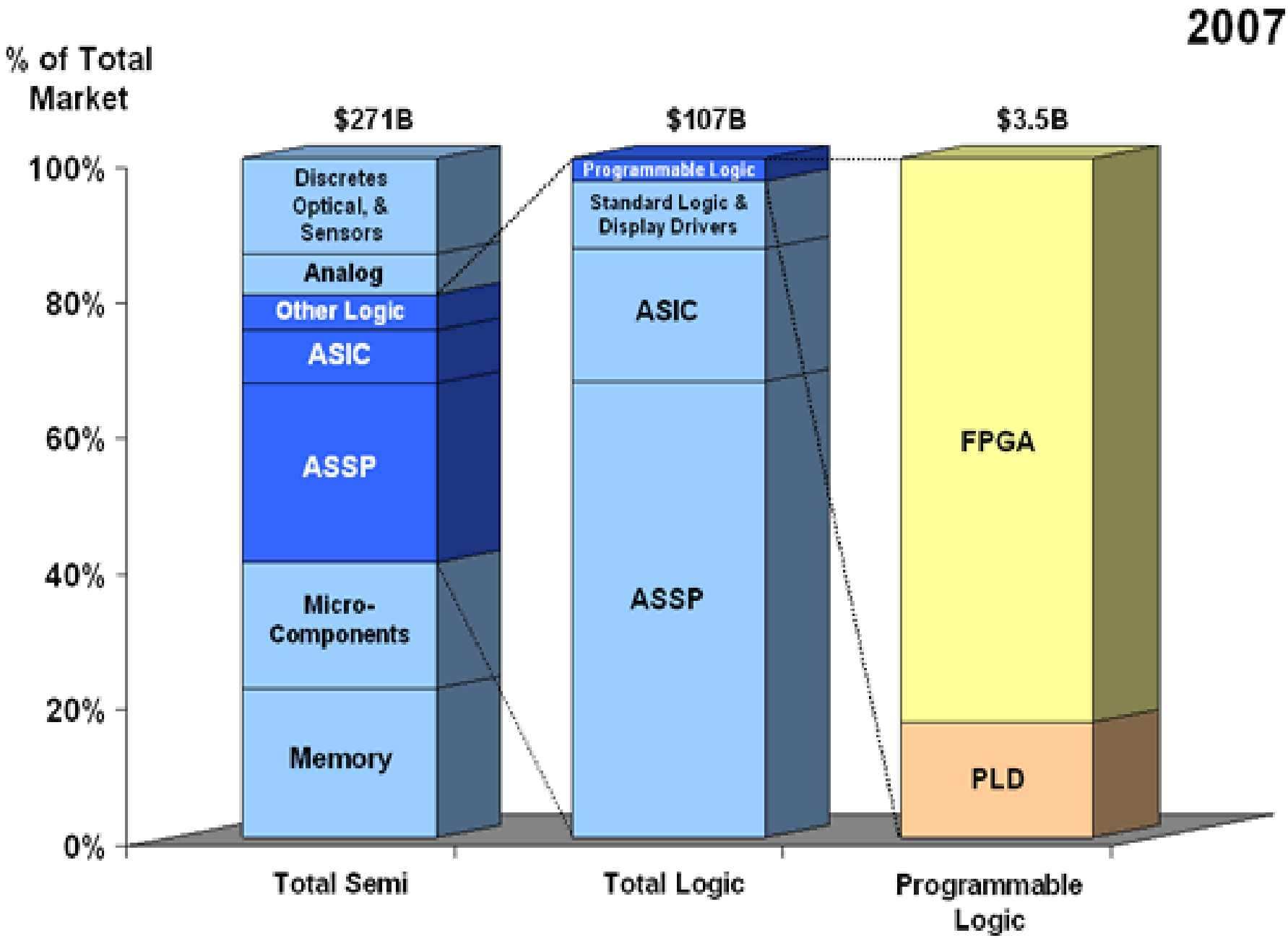
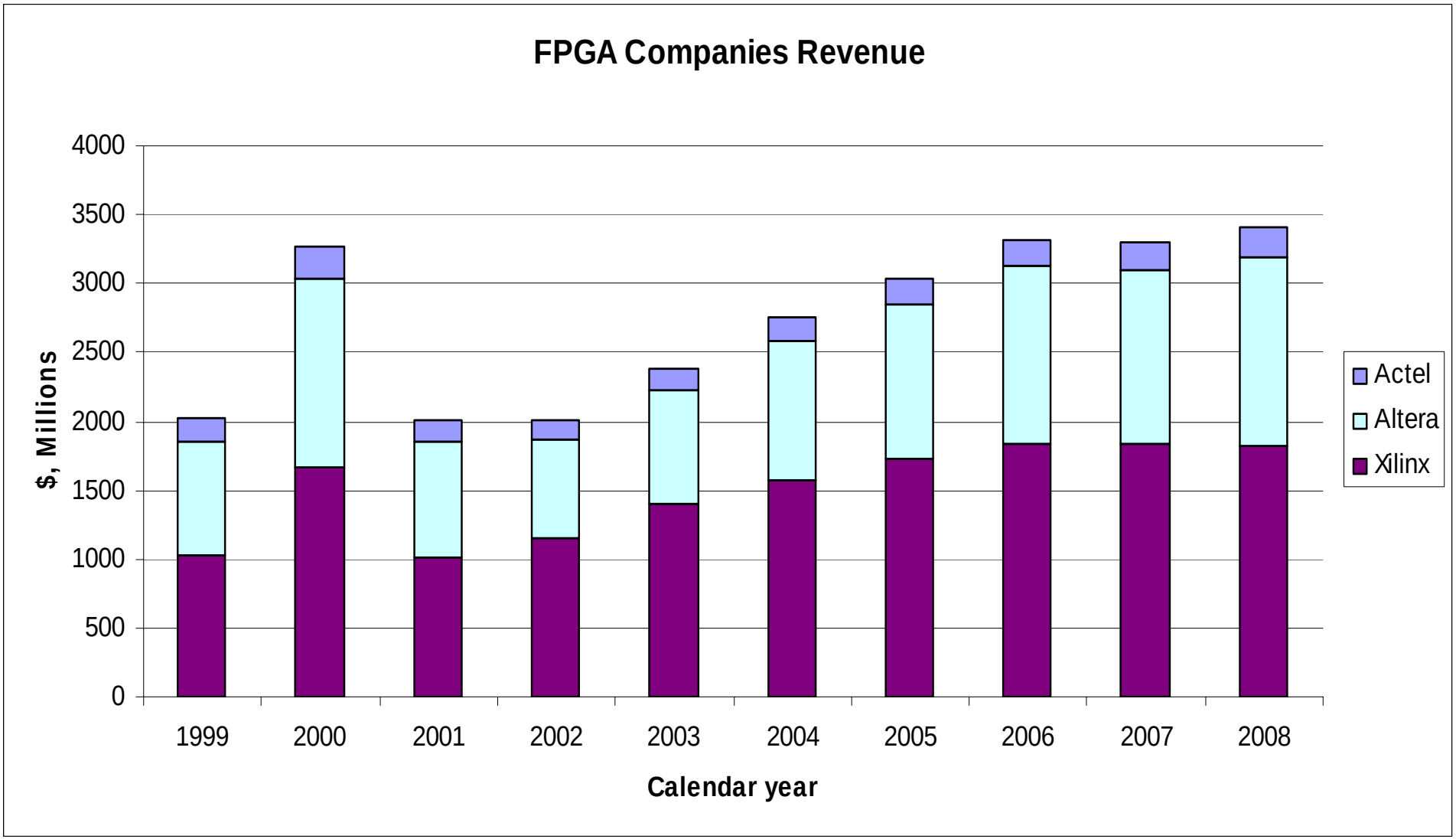
Semiconductor Market



FPGA Aren't Substituting ASIC

Total FPGA Market <$3.5B, No Growth Since 2000



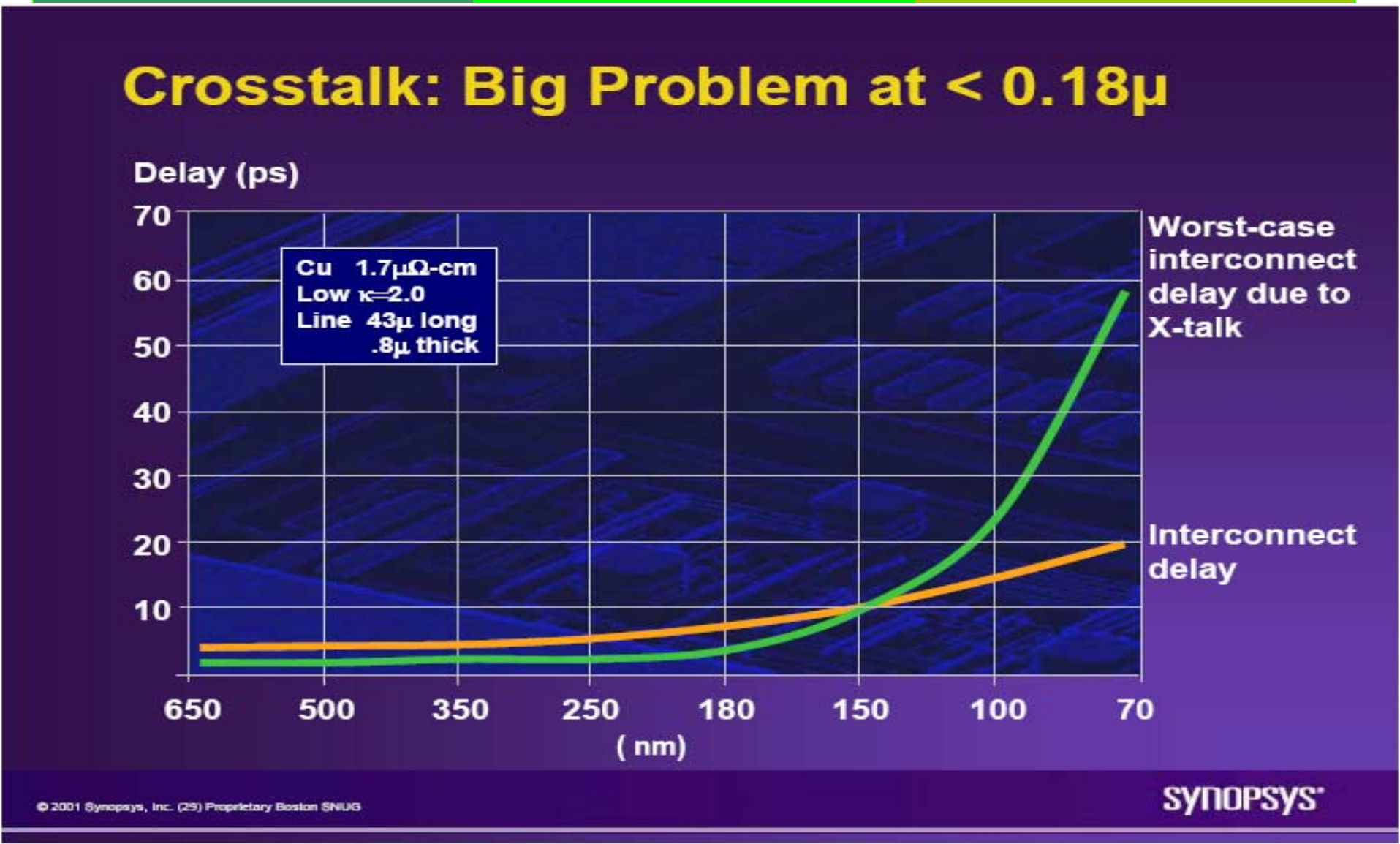
FPGA at ~$4B Clearly didn't Fill the ASIC Gap

FPGA market has barely grown in the last 5 years

- FPGA cost-speed-power make it unattractive for many volume applications
  - FPGA penalty is extremely high *
    - Gate Density: 1: 20-40
    - Power: 1: 9-12
    - Speed: 1: 2-4
- Old Process ASIC is preferable in many applications
  - Density ~1:32=> 5 process generations (45nm FPGA ~ 0.25μ ASIC)
    - => 3-4 gen. older ASIC process (0.13μ-0.18μ) is more competitive
    - => 3-4 gen. older ASIC process fab is fully deprecated and hence cheaper
- ASSP + Software in many cases provide a better alternative

*Ian Kuon and Jonathan Rose, "**Measuring the Gap Between FPGAs and ASICs**", *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems (TCAD)* , Vol. 26, No. 2, pp 203-215, Feb. 2007

And Even Worse: Wire to Wire is Taking Over



The Tyranny of Interconnects

Delay Ratio	**@100nm**		**@35nm**
Routing (1mm)	30ps	6	100
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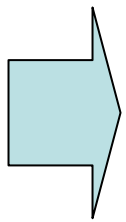
Transistors	5ps	1	1



Power Ratio		
Routing	5	30
	--	---
Transistors	1	1

James Meindl

director of the Microelectronics Research Center at the Georgia Institute of Technology

By Richard Goering EE Times April 19, 2004 (5:00 PM EDT)

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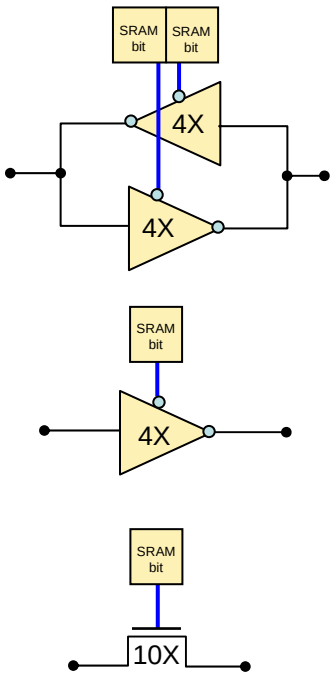
FPGAs see Diminishing Benefits with Scaling

- Over 90% of FPGA logic area penalty is due to programmable interconnect ('PIC')
- Performance and power penalty are direct result of the area
- Transistor as Programmable Interconnect doesn't scale well
- Scaling bring on "The Tyranny of Interconnects"
- Interconnect needs to increase faster than gate count to keep up (Rent's rule)
  - ASIC adds metal layers with scaling
  - PIC limiting factor is the single layer of diffusion shared with the logic.

=> FPGA moved from LUT4 to LUT6-7 as higher granularity logic cells reduce interconnections

Metal to Metal Antifuse Connectivity ~50x Denser than SRAM

SRAM FPGA connectivity elements @ 45 nm

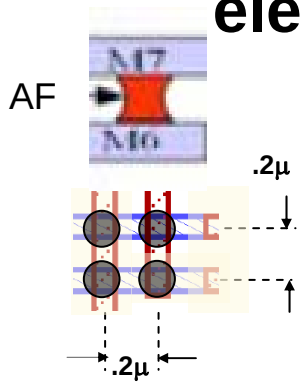


Bidi buffer
Area ≈ 4 μ²
Ratio to AF ≈ 100

TS buffer
Area ≈ 2 μ²
Ratio to AF ≈ 50

Pass gate
Area ≈ .5 μ²
Ratio to AF ≈ 12

Antifuse connectivity element @ 45 nm



Antifuse (AF)

Pitch - 0.2 μ
.2 x .2= 0.04 μ²

Area: 0.04 μ²

FPGAs contain mix of the three elements, with bigger buffer ratio as technology shrinks.

Average area ratio of connectivity element ≈ 50

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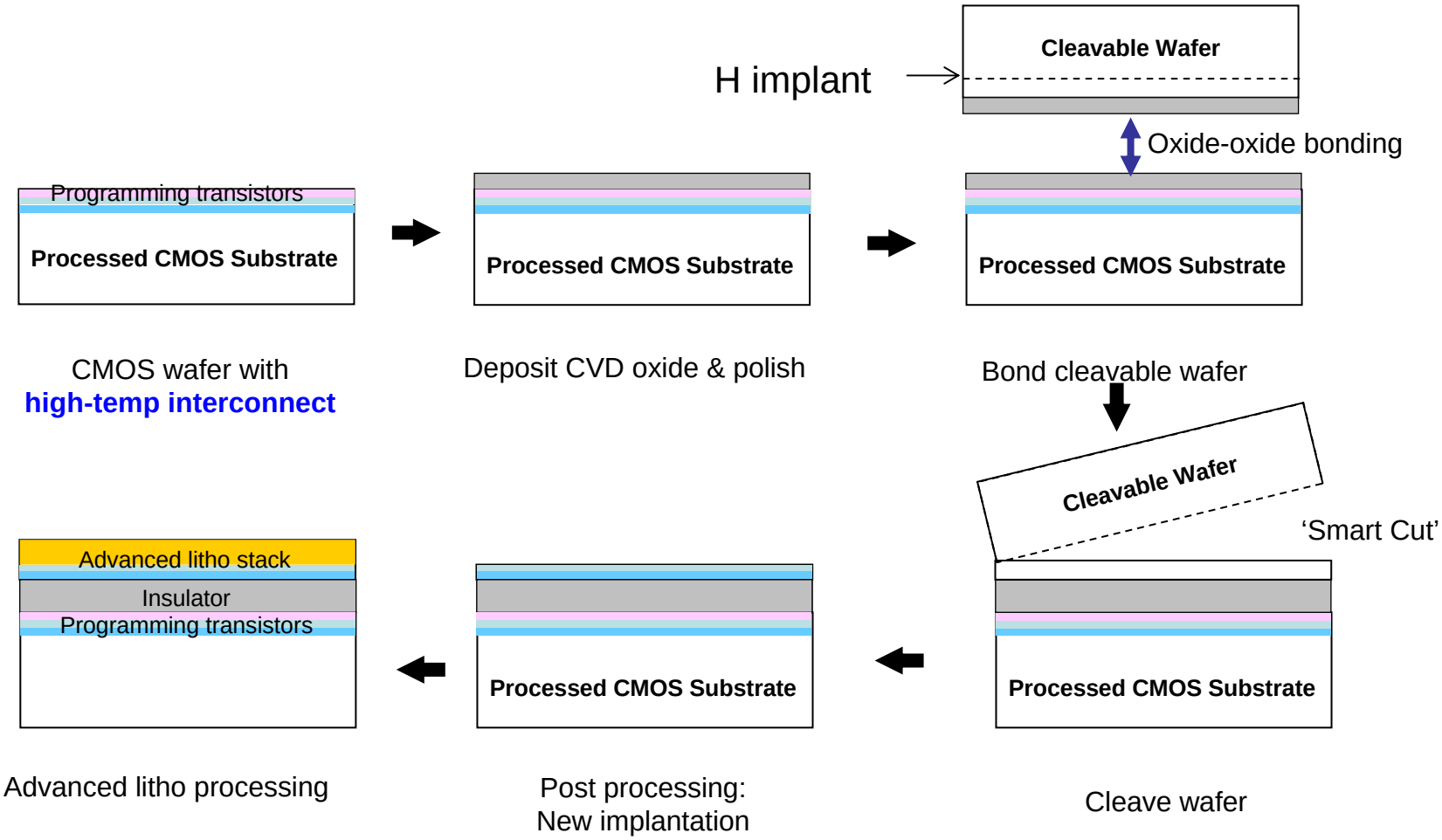
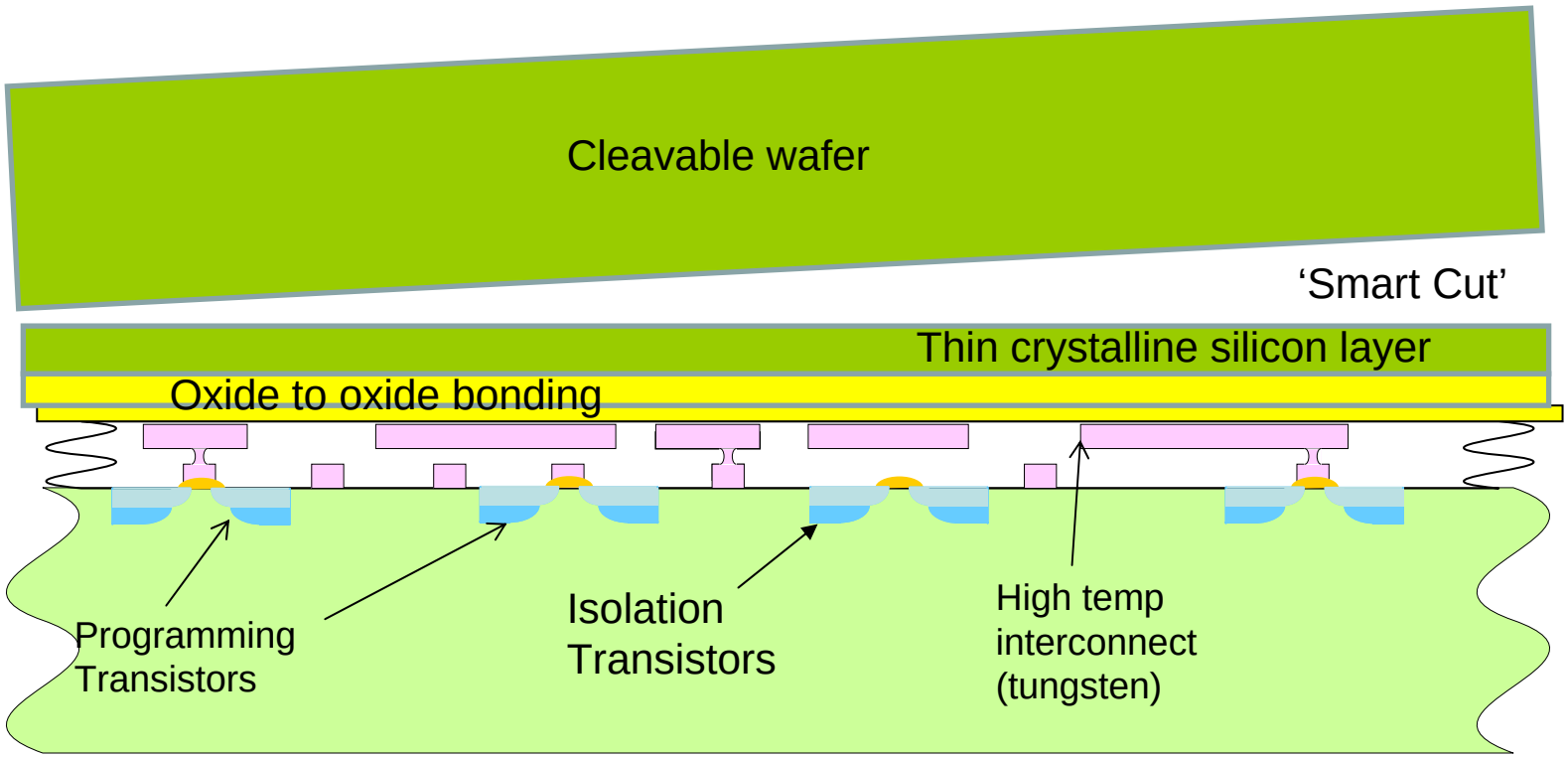
Antifuse Earlier Failure vs. SRAM FPGAs

- SRAM FPGAs were riding the bleeding edge of technology & getting one process node advantage
  - Lesser Importance: Future scaling is expected to slow down
- Re-programmability
  - Lesser Importance: Today even FPGA designs are verified by simulation rather than by trial and error
  - Innovation: Re-programmable antifuse technology
- High Voltage Programming and Isolation Transistors eat away the density advantage
  - 3D Innovation: Programming circuits on another layer

Adding a Thin Crystallized Silicon Layer for the Primary Silicon



Foundation – Pre-fabricated High Voltage Programming Transistors ('Older' Process)



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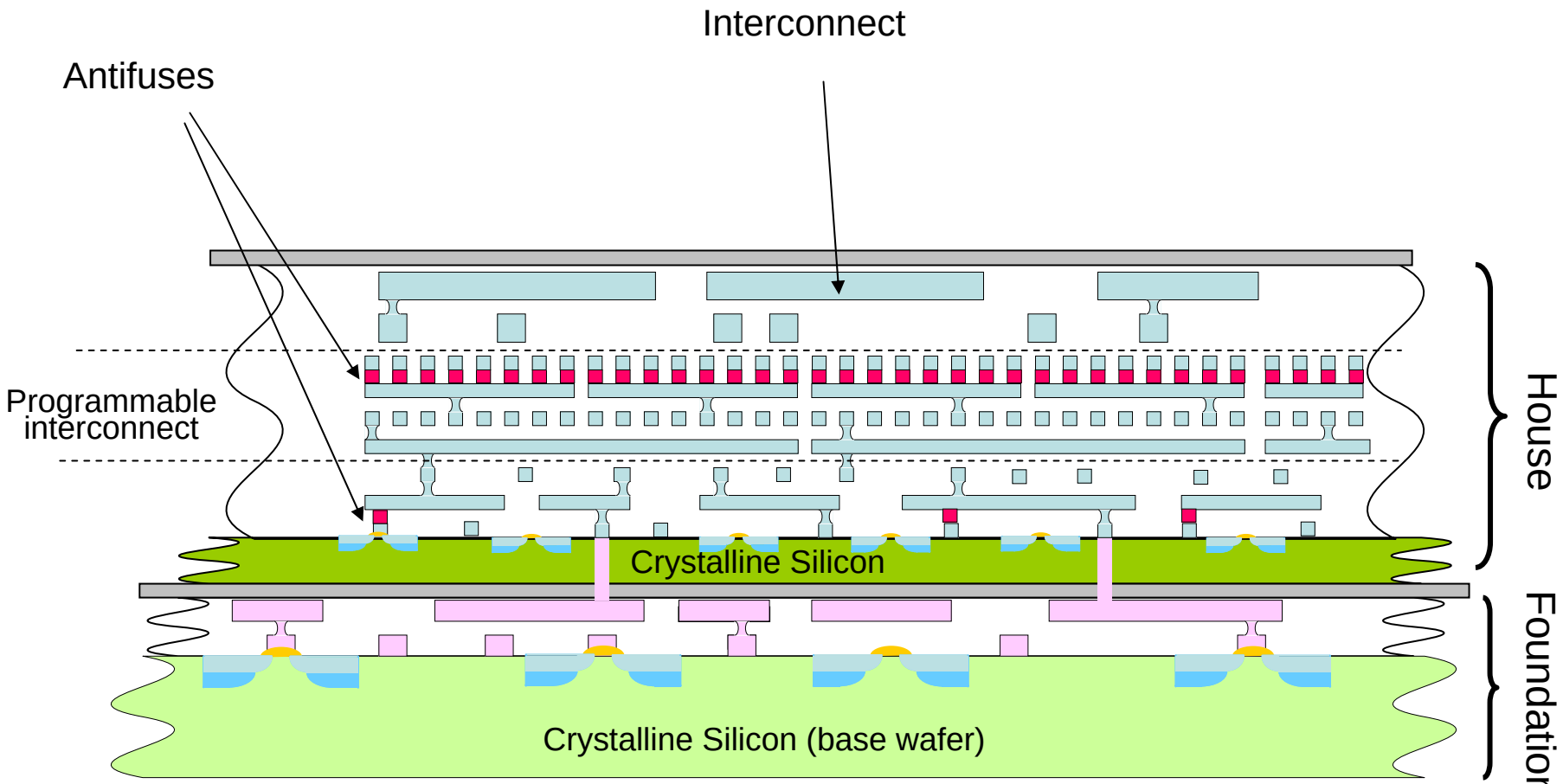
Primary Device (‘House’) on top of the Foundation



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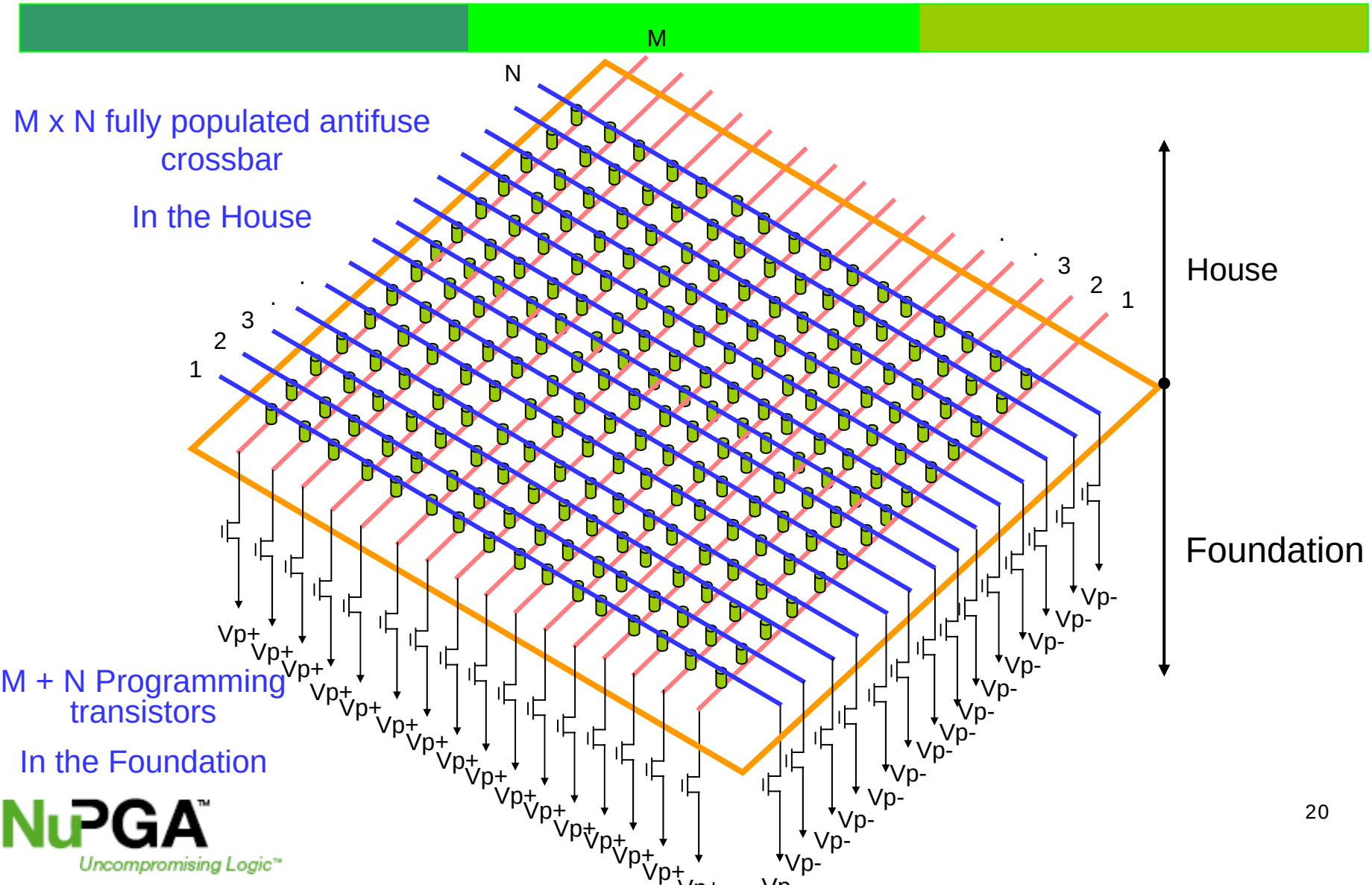
3D Antifuse Connectivity ~ ASIC Connectivity



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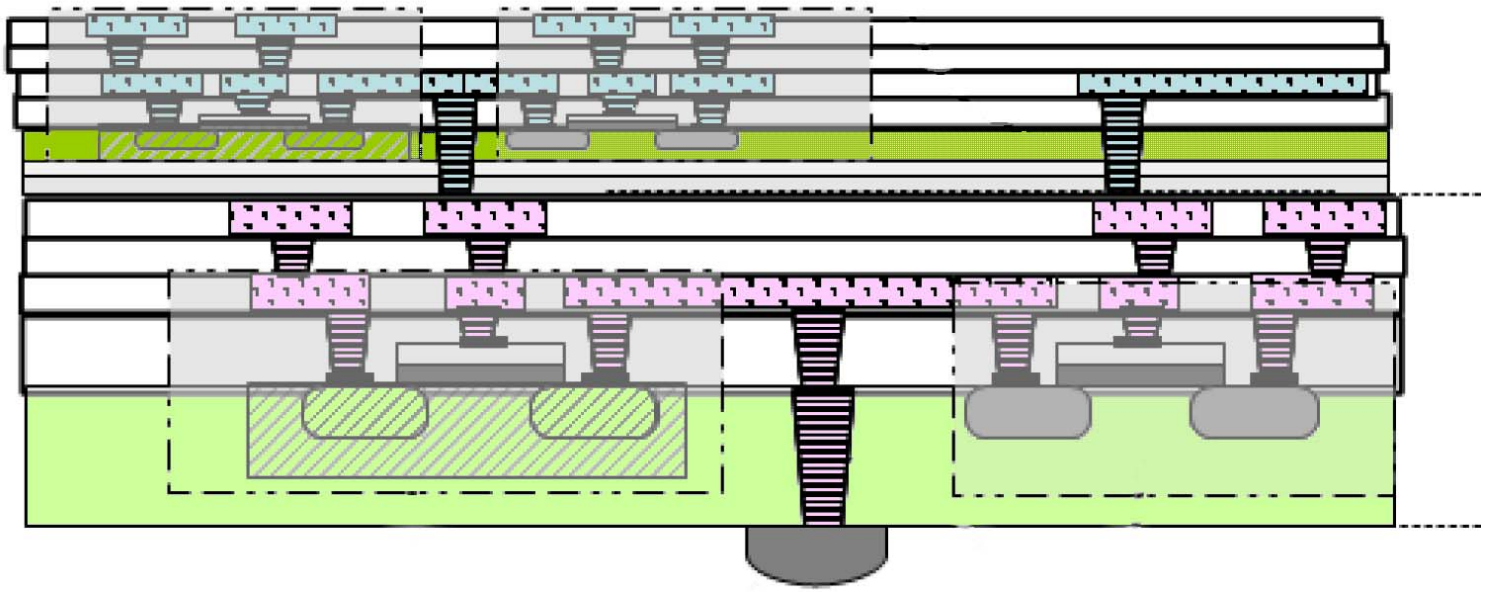
Utilizing The Foundation for TSVs

- TSV + optional redistribution layers are fabricated in the base wafer (‘Foundation’) at low cost process
- Layer transfer – “Smart Cut” to prepare the wafer for subsequent process
- TSV does not consume area of the expensive advanced-process silicon
- Inexpensive method for 3D stacks using TSVs

Using the Foundation for TSV



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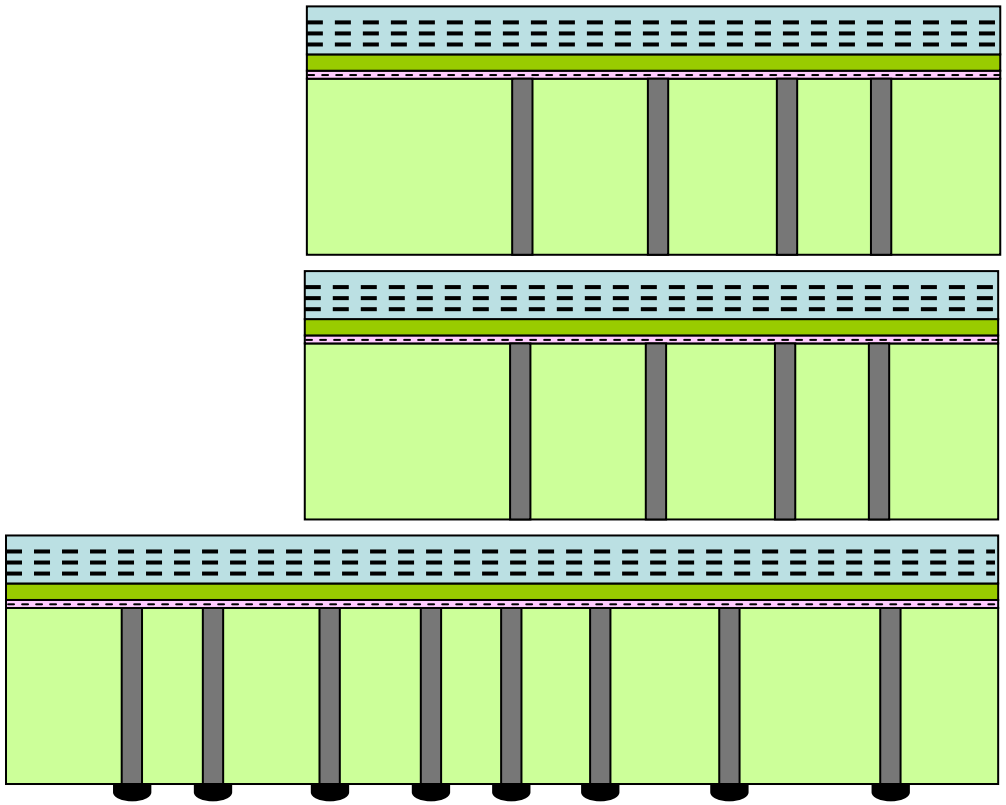
3D IC System with TSVs in the Foundations



3D Processor-DRAM Integrated Systems
The solution to the “Memory Wall” Problem

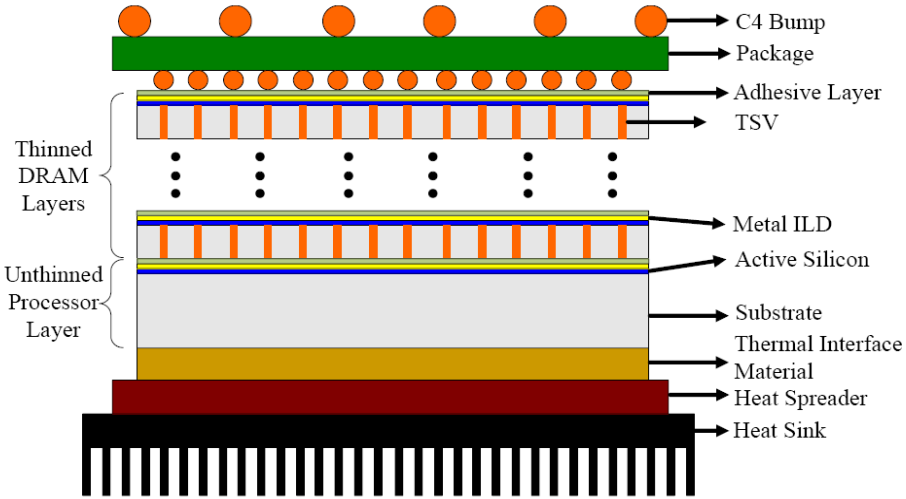
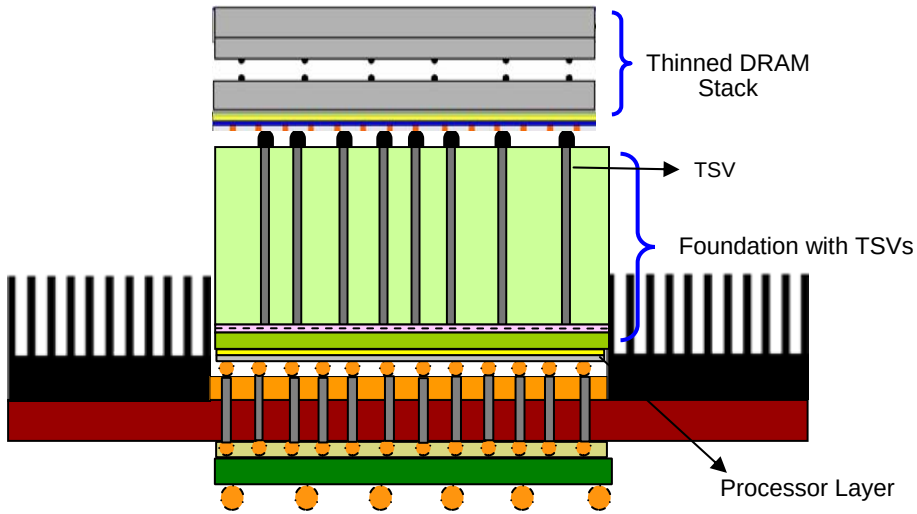


Fig. 1. 3D Processor-DRAM integrated system architecture.

Through-DRAM TSVs* =>

~5% Capacity Degradation

~5% Power Overhead



‘Through-Foundation’ TSVs =>

No DRAM Capacity Degradation

No Power Overhead

Better Processor Power Dissipation

DRAM design independent of Processor design

*Impacts of through-DRAM vias in 3D processor-DRAM integrated systems
Qi Wu; Rose, K.; Jian-Qiang Lu; Tong Zhang
3D System Integration, 2009. 3DIC 2009. IEEE International Conference on

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Summary

- High density custom logic at reasonable NRE is crucial for the industry
- Interconnects are now dominating all logic devices
- The Future is in the Third Dimension – 3D