

Overlay as the key to drive wafer scale 3D integration

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Abstract

3D integration is the stacking of multiple active device layers (with or without interconnecting metal lines) to form a more complex integrated circuit or to provide a new architectural venue. There are many different techniques to accomplish the stacking of the active layers, ranging from packing solutions through wafer bonding, to regrowth of Silicon films. We utilized an aligned SOI wafer bonding method that allows very high alignment accuracy to achieve very dense 3D interconnections. However, wafer bonding tools currently do not have the capability to achieve better than 100 nm overlay error (3 sigma). This limits the highest density we can achieve in a 3D design due to the large landing area that is required to yield the 3D vias, reducing the areal benefit and thus worsening yields. Hence, in this work we will discuss key issues that prevent better than 100 nm 3 sigma alignment between the two substrates. We show that controlled process integration enables significant reduction of the alignment errors between two substrates. The second part of the paper details 3D bonder re-engineering solutions to achieve an order of magnitude improvement in alignment accuracy and drive the full potential of 3DIC. More specifically, inclusion of the learning achieved from lithographic technology, as well as specific bonding process control methods are discussed.

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1. Introduction

3D integration technology employs the stacking of active device layers to form integrated circuits to obtain a higher degree of functionality and performance. First, we will discuss the underlying drivers to pursue 3D integration, followed by a review of aligned wafer bonding methods that enable wafer scale 3D stacking. Finally we will discuss the advantages and challenges of device level 3D integration.

1.1. 3DIC Benefits

Why would one want to stack multiple chips or wafers on top of each other? The advantages of 3D integration are very tempting:

Density improvements: by adding a degree of freedom to wiring and device placement, the packing density increases which can reduce the silicon footprint required by the chip. A variety of areal savings have been reported. From 13% for an N–P split multiplier [1] to 54% for a 32-bit microprocessor design [2].

Performance: It has been shown that wiring delay is increasingly restricting the overall performance of integrated circuits [3]. 3D integration is a very attractive solution to reduce both maximum and average interconnection length. Performance enhancement simulations show 22%

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on a 16×16 bit multiplier [1] and 50% on a 16Mb L2 cache [4]. One implementation shows 400% improvement in the memory bandwidth of a 8051 RISC core on memory [5].

Noise: Longer wires suffer from more noise coupling than shorter ones. Therefore with the decreased average wire length in 3DIC, noise will be reduced. In turn, this allows for fewer repeaters for the global buses, freeing up silicon area and reducing power.

Power: A large part of the total power consumption of an IC is dissipated in the wiring. With the reduction of parasitic capacitance and resistance in a 3DIC, total power will be significantly reduced [1,5,6]

Heterogeneous integration: With 3D integration, traditionally non-compatible substrates can be joined into a monolithic IC. Examples are real-time vision systems [7] and the 8051 core on memory [5].

1.2. Aligned wafer bonding

To enable wafer scale 3D integration, the two substrates require alignment of their patterns during the bonding step. Aligned bonding has been reported as far back as 1990 [8] though the alignment accuracy was several microns. Today, commercial bonders can achieve $\sim 1 \mu\text{m}$ accuracy. This alignment tolerance enables 3D for larger functional blocks. With better alignment accuracy, new applications for 3DIC open up that require high inter-level via densities, for instance device level integration. In the current state-of-the-art aligners a maximum of $\sim 250 \text{ k vias/mm}^2$ can be used. IBM's inter-tier vias have a bottom CD of 140 nm. This allows a maximum via density of $\sim 4 \text{ M vias/mm}^2$. We demonstrated yielding these via connections in a 3DIC [9]. Alignment accuracy directly drives the via density, and therefore the 3DIC application space. The ultimate limit of 3DIC is to allow for 3D circuits with the NFET and PFET devices built on separate wafers, and bond these at the end of the FEOL process. This application drives requirements which currently cannot be met using state of the art aligned wafer bonding.

1.3. The challenge: device level 3D

In state of the art CMOS technology, NFET and PFET devices are processed on a single wafer which often limits their individual performance and complicates integration. Utilization of 3D stacking of NFETs and PFETs layers, to provide “NP-splitting”, would allow simplification by building these two devices on separate wafers, forming two “heterogeneous” substrates. This allows each layer to be optimized for that specific type of device resulting in much better performance and remarkable process simplification. To first order NP-splitting allows the well, extension, halo and source/drain implants to be carried out without masking steps. Further device specific optimizations such as activation anneals, gate oxide thickness, spacers, crystal orientation, stress engineering, or any other options that benefit one device but degrade the other are

made possible with few drawbacks. On the other hand, the active area, gate level and some contacts will be required for both substrates. On the whole, NP-splitting would likely result in slightly more steps to build a wafer pair to Metal 1 than it would in 2D. This larger number of steps implies a yield hit according to Deng [10], but given the significant reduction of chip size made possible by the 3D implementation, yields would roughly be equal to 2D. An additional benefit is the reduced manufacturing time due to the parallel processing of the N and P front-end devices.

2. Enablers for device level 3D

To realize the full potential of wafer scale 3D integration, the alignment of the two substrates needs to surpass the current state of the art in wafer bonding. To meet this challenge, we tailored unit processes and process integration of the 3D stacking to greatly reduce wafer bow which is a large component of the total alignment error. We will also discuss the progress that has been made on the alignment tooling, and future directions to achieve the alignment accuracy required for device level stacking.

2.1. Wafer bonding process

Low temperature bonding can be defined as any bonding process which requires anneal temperatures ranging from room temperature to $400 \text{ }^\circ\text{C}$. Low temperature bonding is required for 3DI to remain compatible with the device and metal wiring processes. For aligned bonding though, the consequences of even low temperature anneals are profound. If heterogeneous substrates are used, elevated temperature can induce as much as $15 \mu\text{m}$ error at $400 \text{ }^\circ\text{C}$ when using Pyrex handle wafers in a front-to-back device stack layer transfer process [11]. For other substrates like GaAs, InP, etc. the difference in CTE to Silicon is greater and would result in more severe alignment issues for bonding at higher temperatures. Therefore we opt for room temperature oxide fusion bonding; thus minimizing the thermal effects. Oxide fusion bonding is chosen over adhesive bonding for two reasons. First of all there is no introduction of non-CMOS-compatible materials in the process that would require extensive work to scale up to a quality and reliability that fits a manufacturing environment. Secondly, the adhesives that have been used by others for 3D stacking [12] are viscous, inducing slip between the two substrates, aggravated by CTE mismatches of the two substrates during the bonding anneal. Our fusion bonding process consists of wafer alignment and tacking at room temperature. No measurable change in alignment is induced during the post-bonding anneal [9].

2.2. Wafer bow control

Bonding alignment is highly sensitive to the shape of the substrates that are aligned. Often, stresses from the films

that are deposited during the processing of the substrates will induce wafer bow. For example in Fig. 1, the substrate bow is given as a function of the process steps. The large variations in wafer bow have a direct impact on the alignment, specifically expansion as is shown in Fig. 2.

The control of film stress on the substrates and introduction of bow-correction steps is of critical importance to minimize the alignment error. With these controls in place, the alignment performance on commercial bonding tools is well within the specifications of the tool. However, to enable the full potential of 3DIC the tool specifications will need to improve by an order of magnitude.

2.3. Wafer alignment systems

In our analysis of the alignment improvements we will use the first few orders of the alignment error description model proposed by Armitage and Kirk [13] to describe the solutions for translation, rotation, wafer expansion and non-orthogonality. As can be seen from Fig. 3, measurements across the wafer are required to appropriately model the factors of the wafer misalignment.

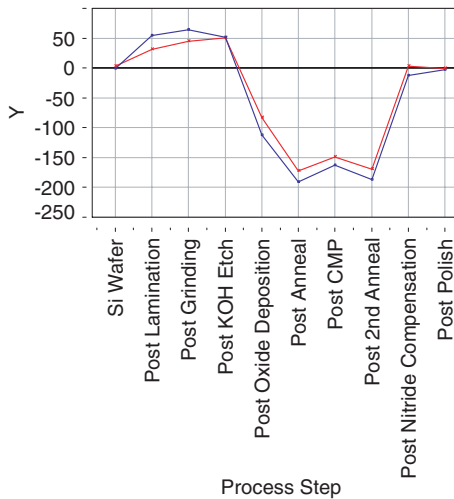


Fig. 1. Wafer bow evolution through several process steps required for 3D integration.

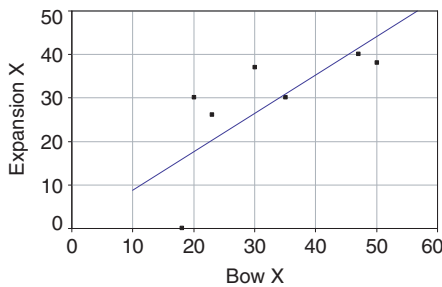


Fig. 2. Relationship between expansion errors and wafer bow after bonding a 200 mm glass handle wafer containing an active circuit layer to a silicon device wafer.

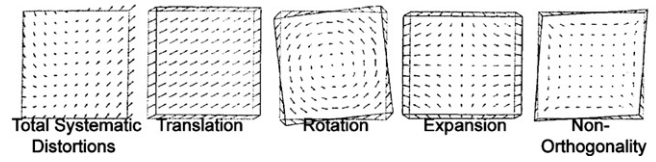


Fig. 3. Total systematic alignment errors, deconvolved into translation, rotation, expansion and non-orthogonality.

The factors in Fig. 3 are routinely dealt with in the lithography world but in the wafer bonding arena technology development driving the alignment accuracy improvements has only just begun. Below, we propose solutions and contrast against other tooling solutions that have been proposed.

2.3.1. Translation and rotation

The translation and rotation errors are mostly determined by measurement capability and the mechanical stability of the system. Commercial tools use image capture and storage to align the two front sides of the substrates. For these systems the stability of the alignment system, as well as the limited data collection limits the alignment accuracy. The image processed, through wafer IR imaging alignment systems described in [14,15] enable better measurement accuracy (± 50 nm). Based on better metrology these two systems achieve alignment accuracy below 500 nm. One major shortcoming is that these two systems are limited by the measurement wavelength ($\lambda > 1 \mu\text{m}$) to maintain transparency of the substrates.

Critical in the aligner is a highly stable system which will determine the final alignment accuracy of translation and rotation.

2.3.2. Wafer expansion

Wafer expansion errors are very sensitive to wafer temperature at the time the bonding occurs. Ideally, both substrates are shot on the same lithography tooling and are at room temperature. The importance of controlling temperature of both substrates independently is shown in Fig. 4. In the graph the expansion error is plotted against the temperature difference of the two substrates to be bonded for

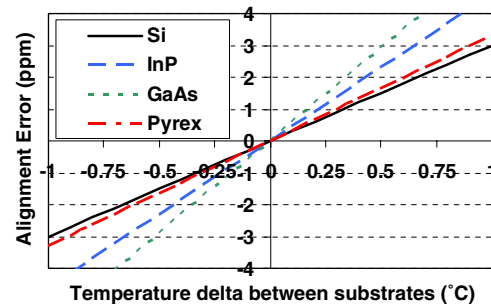


Fig. 4. Expansion errors induced by thermal expansion errors caused by temperature differentials between bonded substrates. The CTE calculation was done for four commonly seen bonding substrates.

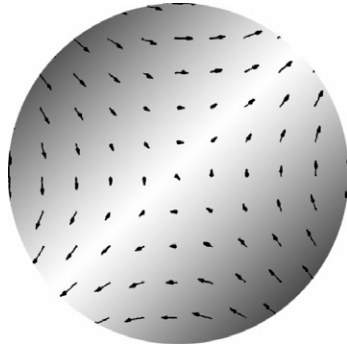


Fig. 5. Non-uniform stage thermal map illustrates a non-orthogonality correction.

different substrates. To achieve the alignment accuracy required for NP-splitting, it is necessary to control substrate temperature to within 0.1 °C.

Also, known expansion errors can be corrected by adjusting the temperature of the aligner chucks. The range of the expansion error correction can cover several parts per million.

2.3.3. Non-orthogonality

Adjusting for non-orthogonality is more complex and requires local variation of the stage temperature to allow orthogonality matching to the companion wafer. In Fig. 5, we show a temperature profile with a qualitative vector map to illustrate this correction capability. The lighter areas indicate warmer areas, and darker areas are cooler. The vectors represent the resulting relative alignment shifts (magnified, of course) following the thermal expansion models described in the previous section.

With the stage heating enabled to correct for the linear components of alignment errors, another improvement becomes possible: local corrections. With the proper metrology, the stage thermal actuators can be driven independently and “nudge” local areas of the wafer small amounts if a non-linear distortion is measured due to wafer pattern placement or localized “slip” of the SOI wafers.

3. Conclusions

Device level wafer stacking, the ultimate 3DIC, can be obtained by process optimization and alignment tool improvements. The process improvements we show allow

better alignment between the two substrates but a key issue remains the alignment tooling. We expect that these requirements will drive the next generation bonding aligners to look more like lithography tooling, utilizing the learning in lithography to achieve the 100 nm alignment tolerance goal. Along with improvements in bonding alignment, metrology capability of the resulting errors requires improvement. Today, no metrology tools can accurately and automatically measure the alignment errors while rework is still possible. These are critical steps towards achieving the full potential of 3DIC and prepare the move from the research lab into manufacturing.

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