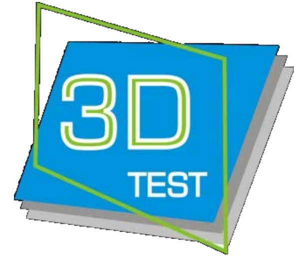
Sixth IEEE International Workshop on Testing Three-Dimensional Stacked Integrated Circuits

3D-TEST



in conjunction with ITC / Test Week 2015
Disneyland Hotel – Anaheim, California, USA
October 8+9, 2015
http://3dtest.tttc-events.org

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Call for Participation

The 3D-TEST Workshop focuses exclusively on test of and design-for-test for three-dimensional stacked ICs (3D-SICs), including Systems-in-Package (SiP), Package-on-Package (PoP), and especially 3D-SICs based on Through-Silicon Vias (TSVs), micro-bumps, and/or interposers. While 3D-SICs offer many attractive advantages with respect to heterogeneous integration, smaller form-factor, higher bandwidth and performance, and lower power dissipation, there are many open issues with respect to testing such products. The 3D-TEST Workshop offers a forum to present and discuss these challenges and (emerging) solutions among researchers and practitioners alike.

3D-TEST will take place in conjunction with the IEEE International Test Conference (ITC) and is sponsored by the Test Technology Technical Council (TTTC) of the IEEE Computer Society.

Workshop Program – The workshop program contains the following elements.

- Keynote Addresses:
  - "New Paradigm Shift in 3-D Design and Testing" by Jeff Rearick – AMD, USA
  - "3D Integrated CMOS-Memristor Hybrid Circuits: Devices, Integration, Architecture, and Applications" by K.-T. (Tim) Cheng – UC Santa Barbara, USA
  - "Known Good Die – Fantasy Land or Tomorrow Land?" by John Carulli and TM Mak – GLOBALFOUNDRIES, USA
- Four sessions with in total 13 paper presentations.
- Two panel-discussion sessions
  - Monolithic 3D: Will It Happen and If So, What Are The Test Challenges and Solutions?
  - Test Model Generation for JEDEC 3D Memories: Who Owns the Responsibility?
- Continuous display of table-top demos.

For the detailed version of the program, please turn over.

Participation – You are invited to participate in the workshop. Participation requires registration and a registration fee. Workshop registration includes access to all technical sessions, Electronic Workshop Digest (containing extended abstracts, papers, slides, posters, as made available by their presenters), workshop reception, continental breakfast, lunch, and break refreshments. On-line registration is available via the workshop's website (http://3dtest.tttc-events.org). Alternatively, register on-site during Test Week at the ITC Registration Counter at the Disneyland Hotel; admission for on-site registrants is subject to availability.

Further Information

Yervant Zorian
General Chair
Synopsys
700 East Middlefield Road
Mountain View, CA, USA
tel. +1 (650) 584-7120
yervant.zorian@synopsys.com

Erik Jan Marinissen
Program Chair
IMEC
Kapeldreef 75
B-3001 Leuven, Belgium
tel. +32 16 28-8755
erik.jan.marinissen@imec.be

Shi-Yu Huang
Program Vice-Chair
National Tsing-Hua University
101, Sec. 2, Kuang-Fu Road
HsinChu, Taiwan
tel. +886 3-573-1147
syhuang@ee.nthu.edu.tw

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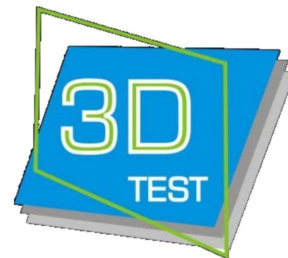

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Workshop Program

Thursday October 8, 2015

Session 1: Opening

Moderator: ChoonLeong Lou – STAr Technologies, TW

16:00h: **Welcome Address**
General Chair: Yervant Zorian – Synopsys, USA
Program Chair: Erik Jan Marinissen – IMEC, BE
Program Vice-Chair: Shi-Yu Huang – National Tsing-Hua University, TW

16:15h: **Keynote Address**:
New Paradigm Shift in 3-D Design and Testing
**Jeff Rearick – Sr. Fellow – AMD, US*
Bryan Black, Michael Alfano – AMD, US; Peter Li, Anson Li – AMD, CN

2.5D/3D ASIC design became a reality when AMD introduced Fiji-based products in the market. The tremendous power/performance benefit generated by this technology is very well received. Testing of such a complex design is a big challenge. Several key design/test challenges will be discussed including the overall DfT architecture, KGD, and test flow.

Session 2: Test Flow Optimization

Moderator: Marc Hutner – Teradyne, USA

16:45h: Test Flow for Advanced Packages (2.5D/SLIM/3D)
Gerard John – Amkor Technology, USA

17:05h: Test-Flow Selection for 3D-Stacked ICs: Theoretical Basis, Optimal Search, and Solutions with Computable Approximations
*Mukesh Agrawal – Intel, USA; *Krishnendu Chakrabarty – Duke University, USA*

17:25h: 3D-COSTAR: A Tool for 2.5D/3D Test Flow Optimization
*Mottaqiallah Taouil, Said Hamdioui – TU Delft, NL; *Erik Jan Marinissen – IMEC, BE*

Session 3: 3D-Memory Test Models: Panel Discussion

17:45h: **Test Model Creation for JEDEC 3D Memories: Who Owns The Responsibility?**

Moderator: Sampath Karikalan – Sr. Manager Package Engineering – Broadcom, USA

Panelists:
Jonathon E. Colburn – Distinguished Engineer – nVidia, USA
Ken Ferguson – Technical Director TTE – PMC-Sierra, CAN
Marc Greenberg – Director Product Marketing DDR Controllers – Synopsys, USA
Hongshin Jun – Research Fellow – SK hynix, KR
Christos Papameletis – Lead DfT Engineer – Cadence Design Systems, USA

Memory-on-logic stacks are among the first 3D products on the market. JEDEC standardizes both stand-alone and stackable memories. Although JEDEC standards for stackable memories include certain DfT features, testability and flow requirements for stack-level testing are seldom considered during the standardization phase. A critical example is the test-model of the memory: ATPG tools require a structural Verilog model for the die/block in order to generate patterns, while such a model is never part of the JEDEC standard. Who should create the model? The memory maker? The stack integrator? Or the EDA supplier? How to ensure that the model matches the standard as well as the specific DRAM implementation? This panel discuss this issue from all angles.

Workshop Reception

19:00-21:30h

Friday October 9, 2015

Workshop Breakfast

07:00-08:00h

Session 4 : Invited Keynotes

Moderator: Dave Armstrong – Advantest, USA

08:00h: **Keynote Address**:
3D Integrated CMOS-Memristor Hybrid Circuits: Devices, Integration, Architecture, and Applications
K.-T.(Tim) Cheng – Associate Vice Chancellor, Professor – UC Santa Barbara, USA

I will give an overview of our recent research efforts on monolithic 3D integration of CMOS and memristive nano devices. These proposed hybrid circuits combine a CMOS subsystem with multiple layers of nanowire crossbars, consisting of arrays of two-terminal memristors, all connected by an area-distributed interface between the CMOS subsystem and the crossbars. This approach combines the advantages of CMOS technology with the extremely high density of nanowires, nano devices, and interface vias. As a result, the 3D hybrids could potentially overcome limitations pertinent to other 3D integration techniques and enable unprecedented memory density and bandwidth at manageable power dissipation, along with other new applications.

08:30h: **Keynote Address**:
Known Good Die – Fantasy Land or Tomorrow Land?
**John Carulli, TM Mak – GLOBALFOUNDRIES, USA*

The term KGD has been thrown around as if there is a magic wand that can identify good die from bad prior to final system configuration. Probing has been used to allow a temporary interconnect from the die to the test instrumentation for this early “goodness” assessment of functionality and specification conformance. However, temporary implies that there will be some limiting characteristics compared to a permanent system implementation. For complex SOCs, performance, power, and IP integration are increasing. This is driving more bumps, thinner probes, lighter force, less contact area, more contact resistance, and less mechanical strength. Can we continue to emulate package/system-level tests to cover full function, performance, and power via full contacting approaches? Are there other approaches that may not require KGD at all?

Session 5: Test and DfT for Real 3D-SIC Products

Moderator: Eric Hill – Cascade Microtech, USA

09:00h: A Review of Test Challenges with Xilinx's 3D IC
**Shahin Toutounchi, Steve Jeong – Xilinx, USA*

09:25h: HBM Test Challenges and Solutions
**Hongshin Jun, Sangkyun Nam, Jong-Chern Lee, Yong Jae Park, Jae Jin Lee – SK hynix, KR*

09:50h: High-Performance HBM Known Good Stack Testing
**Marc Loranger – FormFactor, USA; John Oonk – Teradyne, USA*

Session 6: Table-Top Demos

10:15h: For list of Table-Top Demos: see next page.
Coffee and tea provided.

Session 7: Monolithic 3D: Invited Talk + Panel Discussion

Moderator: Françoise von Trapp – “Queen of 3D” – 3DInCites, USA

10:45h: Monolithic 3D is Already Here – the 3D NAND – and Now Would be Easy to be Adapted for Logic
Zvi Or-Bach – MonolithIC 3D, USA

We will review what have been the barriers to monolithic 3D and how these barriers could now be overcome by re-inventing the 20-year old ELTRAN process. The modified ELTRAN process enables any fab using its existing equipment and transistor process to build a two-layer monolithic 3D device. We will show how adding the newly released precise bonder into the fab would enable unlimited number of layers, allowing wide-range of mixing options for sequential and parallel process options. Finally we will point out for some unique testing challenges that arise from these new semiconductor capabilities, such as contactless in-process testing, and per-layer testing.

11:00h: **Panel Session: Monolithic 3D: Will It Happen and If So, What Are The Test Challenges and Solutions?**

Panelists:
Yang Du – Director Engineering – Qualcomm Research, USA
Sandeep K. Goel – Academician/Senior Manager – TSMC, USA
Zvi Or-Bach – CEO – MonolithIC 3D, USA
Bob Patti – CTO – Tezzaron Semiconductor, USA
Sebastien Thuriès – Research Engineer – CEA-Leti, FR

In a Monolithic 3D (M3D) stack, circuit layers are grown sequentially on top of each other, rather than bonded as pre-fabricated dies as in the conventional 3D-SIC paradigm. M3D offers less alignment issues, higher density interconnects, and improved performance since large through-silicon vias are replaced by small inter-tier vias similar to conventional vias. However, all these benefits do not come without critical challenges. These include sub-optimal performance of transistors grown in upper layers, thermal issues, optimal bonding temperature, and most importantly how to apply the KGD concept. This panel discusses these challenges and brainstorms with the audience about the possible solutions.

Workshop Luncheon

12:00-13:00h

Session 8: EDA for 3D-TEST

Moderator: Benoit Nadeau-Dostie – Mentor Graphics, CAN

13:00h: At-Speed Inter-Die Interconnect Test in 2.5D- and 3D-SICs
Konstantin Shibin – Cadence Design Systems, DE;
*Vivek Chickermane, Brion Keller, *Christos Papameletis – Cadence Design Systems, USA;*
Erik Jan Marinissen – IMEC, BE

13:25h: IEEE 1687 TAP-Based 3D-DFT Architecture for Testing Multi-Chips Active Interposer System
*Pascal Vivet, Jean Durupt, *Sebastien Thuriès – CEA-Leti, FR;*
Jürgen Schlöffel, Mentor Graphics, DE

13:50h: Synopsys 3D Test Technology Glut
**Adam Cron, Gurgen Harutyunyan – Synopsys, USA*

Session 9: Research in 3D-TEST Wonderland

Moderator: Michael Wahl – University of Siegen, DE

14:15h: Testing of the Clock Networks in 3D ICs
*Shao-Fu Yang, *Shi-Yu Huang – National Tsing Hua University, TW;*
Kun-Han Tsai, Wu-Tung Cheng – Mentor Graphics, USA

14:40h: Power-Supply-Noise-Aware Timing Analysis and Test Pattern Regeneration for Low Power 3D IC
*Cheng-Yu Han, Yu-Ching Li, Hao-Tien Kan, and *James Chien-Mo Li – National Taiwan University, TW*

15:05h: Learning-Based Reliability Management for Dark Silicon Systems
**Taeyoung Kim, Xin Huang, Sheldon X.-D. Tan – University of California at Riverside, USA;*
Valeriy Sukharev – Mentor Graphics, USA

15:30h: Dual-Duty Redundant TSVs Design and Allocation for 3D ICs
*Pu Pang – Shanghai Jiao Tong University, CN; Xu He – National University of Defense Technology, CN; Yuchun Ma – Tsinghua University, CN; *Li Jiang – Shanghai Jiao Tong University, CN*

15:55h: Workshop Closure

16:00h: End

* = speaker

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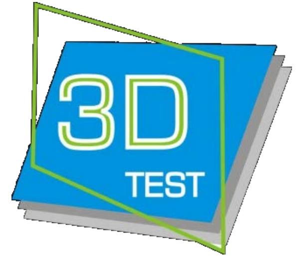

Table-Top Demos

Table-Top Demos

Table-Top Demos are on display throughout the workshop.
Dedicated demo session

- Friday October 9: 10:15-10:45h

Demo 1: Analysis of Advanced Semiconductor IC Devices Using Terahertz Frequency Technology
Stuart Neches – Advantest America, USA

Demo 2: 3DIC Parametric and Reliability Qualification with STAr Gemini ATE and Aries Vertical Probe Card
Nick Gullett – Semiconductor Consultants, STAr Technologies, USA

Demo 3: Synopsys 3D Test Technology Glut
Adam Cron, Gurgen Harutyunyan – Synopsys, USA

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