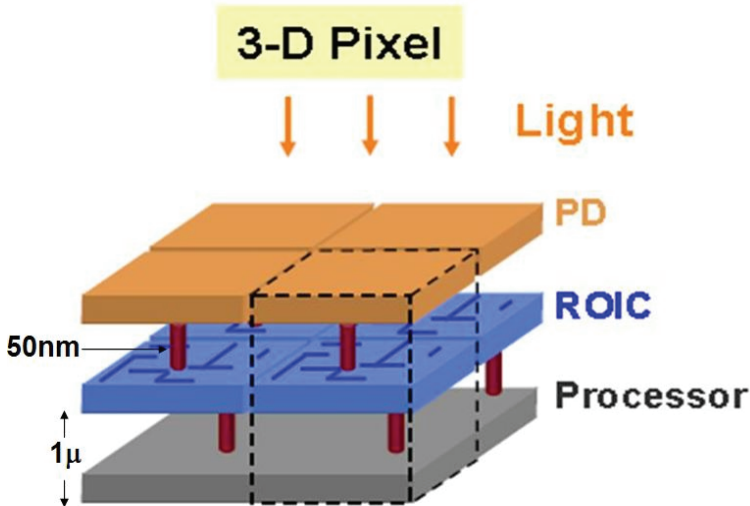




Technology Breakthrough

Multi-Spectrum Imager with Vertically Integrated Processor



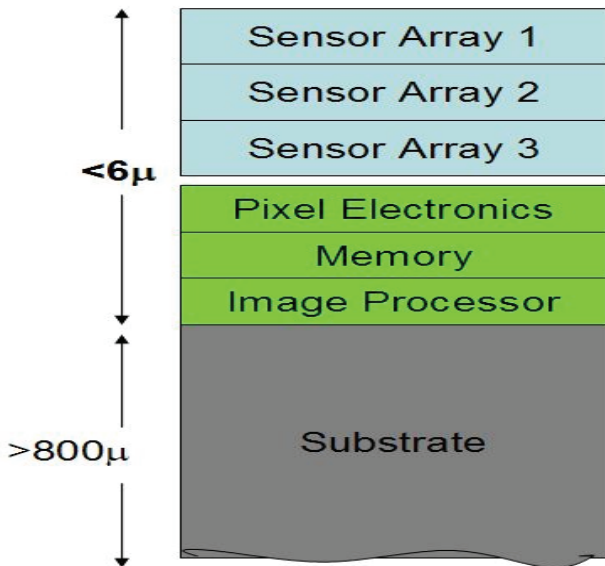
Technology:

The monolithic 3D IC technology is extended by adding multiple image sensors layers. Monolithically integrating CMOS signal processing array with multiple layers of image sensor with very rich vertical interconnects.

Key Features:

- Vertical interconnect pitch <100nm
- Typical strata thickness <1µ

See reverse side for more on monolithic 3D IC technology



Benefits:

- Visible and infrared sensors integrated in a single stack – Day/Night capability in one stack.
- Multi-spectrum Imager
- Extremely high dynamic range
- Extremely high speed capturing
- High resolution
- Dramatic reduction in power, size and cost

Imager Options:

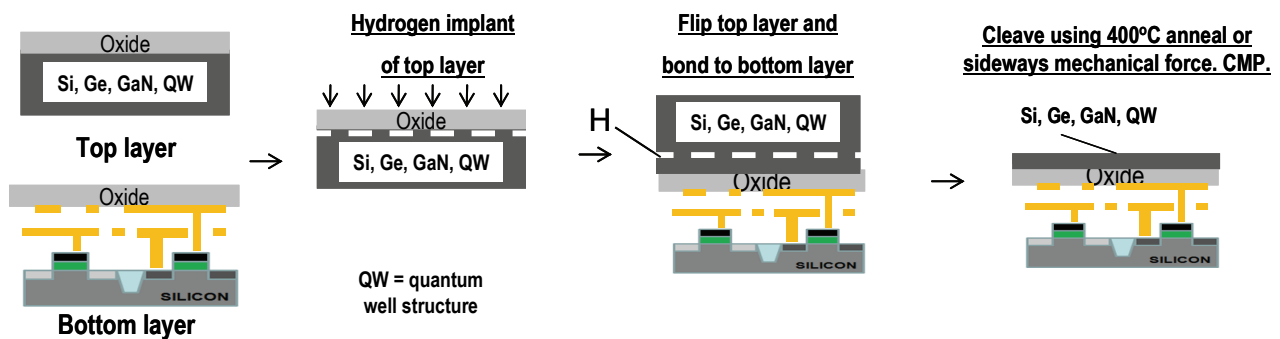
	Multi Spectrum	Day/Night	Light/Shadow	Your Application
Sensor Array 1	Spectrum 1	N/A	N/A	
Sensor Array 2	Spectrum 2	Night Sensor Array	Low Sensitivity	
Sensor Array 3	Spectrum 3	Day Sensor Array	High Sensitivity	

Layer Transfer Technology (“Ion-Cut”)

Defect-free single crystal obtained @ <400°C

Leveraging a mature technology (wafer bonding and ion-cleaving) that has been the dominant SOI wafer production method for over two decades.

Innovate and create multiple thin (10s – 100s nanometer scale) layers of virtually defect free Silicon, Germanium, Gallium Nitride, and quantum well structures by utilizing low temperature (<400°C) bond and cleave techniques, and place on top of active transistor circuitry. Benefit from a rich layer-to-layer interconnection density.



Create a layer of Recessed Channel Transistors (RCATs), commonly used in DRAMs, by activating dopants at ~1000°C **before** wafer bonding to the CMOS substrate and cleaving, thereby leaving a very thin dopant stack layer from which transistors are completed, utilizing less than 400°C etch and deposition processes.

