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Building blocks for wafer-level 3D integration

Executive OVERVIEW

The microelectronic industry has arrived at a crossroads. There is the challenge of continued Moore's Law scaling and the ever-growing consumer demand for smaller, faster electronics with extended and new functionalities. 3D integration is a promising and fast-growing field that addresses the convergence of Moore's Law and more than Moore. 3D integration offers a path for higher performance, higher density, higher functionality, smaller form factor, and potential cost reduction. Through this emerging field, new and improved technologies and integration schemes will be necessary to meet the associated manufacturing challenges. With the possibility of addressing different process flows, this paper describes 3D building blocks, including stacking technology as well as a low temperature layer transfer technology and a metal-to-metal bonding technique.

Mariam Sadaka, *Soitec USA Inc., Austin, TX USA;* **Lea Di Cioccio**, *CEA-DRT-LETI , Grenoble, France*

The emerging field of 3D integration aims at providing highly integrated systems by vertically stacking and connecting various materials, technologies, and functional components together. Furthermore, potential 3D integration benefits come from the higher interconnect density, shorter wire lengths, and small chip size. Based on this, advances in 3D integration are gaining significant momentum and have become of critical interest to the semiconductor industry as a promising path to achieve further improvement in IC performance.

In this article, we are focusing on low temperature wafer bonding, including oxide-oxide and metal-metal bonding, as well as low temperature layer transfer as critical building blocks for IC wafer-level stacking.

The stacking technology

Smart Stacking is a wafer-to-wafer stacking technology platform of partially or fully processed wafers (**Fig. 1**). This technology enables transferring of very thin layers in a high-volume production environment. The core technologies are low temperature molecular oxide-oxide bonding, surface conditioning, and wafer thinning. This technology is adapted for advanced semiconductor applications, such as back-side illumination (BSI) image sensors as well as via last 3D integration approaches [1,2,3]. The technology platform scales from 100 to 300mm wafer diameter and is compatible with various wafer types (e.g., Si, glass, fused silica, poly SiC).

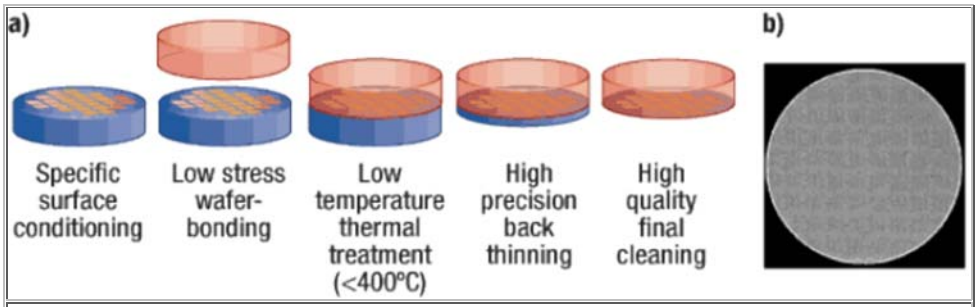
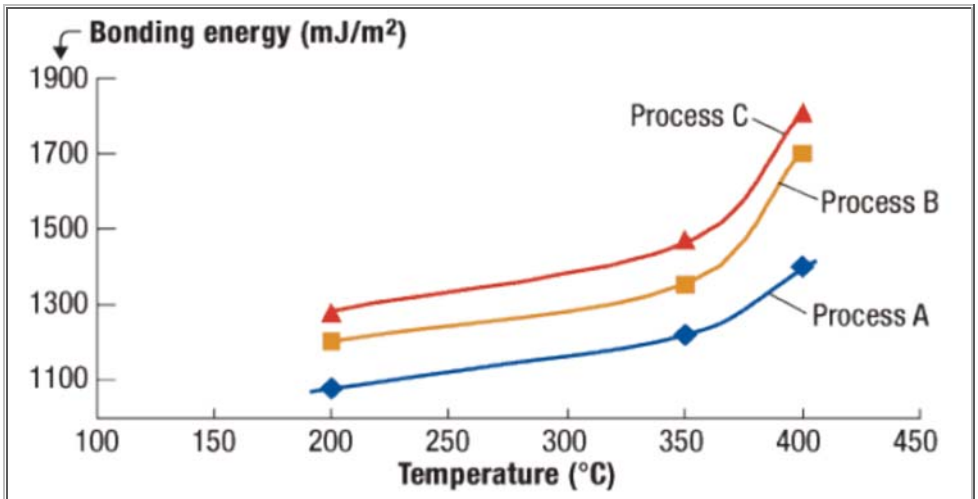


Figure 1. Process schematic of the Smart Stacking technology (a); Acoustic microscope of typical wafer with reduced edge exclusion (b).

Direct bonding of two oxide surfaces requires considerable control of surface properties— topology, flatness, micro-roughness, edge roll-off, bow, and warp—as well as particle contamination and surface chemistry in order to achieve high-quality bonding. Wafer topology is controlled by a chemical-mechanical polishing process that maintains wafer edge quality, and wafer micro-roughness needs to be in the range of 0.25nm RMS [4, 5]. Accordingly, the new stacking technology incorporates know-how and expertise in surface preparation, cleaning, and high-precision wafer planarization techniques yielding a low defectivity process (Fig. 1b).

To address the thermal budget constraint imposed by stacking of back-end of line processed wafers (i.e., <400°C), specific pre-bonding surface conditioning and post-bonding thermal treatment were developed to control and increase the bonding strength within the reduced thermal budget window. Although the wafer direct bonding takes place at room temperature, the thermal treatment is done at a temperature between 200°C and 400°C. Bonding strengths are measured by Maszara's blade technique [6], showing significant increase in bonding strength at low temperature (**Fig. 2a**). The data show that, with appropriate pre-bonding surface conditioning, high bonding energies

compatible with aggressive wafer grinding and thinning processes can be achieved even after low temperature treatments.



Test	Condition	Pass/fail
Operating life test (endurance)	125°C/2000h	√
High temperature storage	150°C/1000h	√
Temperature cycling	-55°C, +125°C, 15°/min	√
Moisture resistance	65°C, -10°C, 90-100% RH-10 days	√

Figure 2. Low temperature oxide-oxide bonding showing high bonding energies with optimized pre-bonding surface conditioning (a); Reliability results for BSI image sensors (b). Also passed: vibration, mechanical shock and pull test (Courtesy of e2v).

Unlike adhesive or thermo compressive bonding, the direct low temperature oxide bonding maximizes throughput and eliminates contribution of wafer thermal expansion. Therefore, the possibility of adding stress to the bonded wafers, thereby impairing devices and interconnects and inducing wafer deformation using the new stacking process, are diminished or avoided. Reducing process-induced distortion is key to avoiding a yield or reliability impact as well as improving critical alignment accuracy. The new stacking technology is being commercially applied to build backside-illuminated (BSI) image sensors, and is compliant with military reliability standards [MIL-STD883] (Fig. 2b).

After the processed wafers are bonded, the next step includes precision grinding, and chemical and mechanical thinning with controlled uniformity. The thinning processes can achieve a thickness of a few microns for a bulk donor wafer, but when combined with the etch stop layer of an SOI wafer, it can achieve thicknesses of <1.0µm with a silicon uniformity of ±7.5nm. When circuits are built on SOI wafers, the buried oxide acts as a built-in etch stop as well as protection for the active Si layer (SOI layer) during the substrate removal process.

When SOI wafers are used, the active Si layer can be ultra thin, and the overall thinning process becomes less complex and more robust due to a more uniform thinning. The thinner Si contributes to a smaller through-silicon via (TSV) aspect ratio, which enables scaling to smaller TSV diameters and higher TSV density. This satisfies the ITRS trend for high-density TSV specification [7]. Moreover, the buried oxide prevents crystal defects from impacting the active layer—a key advantage for high reliability 3D systems.

The layer transfer technology

While Smart Cut [8] is used for SOI production, it also includes the transfer of a blanket layer, including single crystal Si film, onto a processed wafer. On this new material layer, a second level of devices can be processed, and this integration can be repeated in an iterative mode. This approach is enabled by a low temperature layer transfer compatible with back-end-of-line processes. In this particular application, the technology includes molecular bonding followed by atomic level cleaving of silicon based on light species implantation (**Fig. 3**). This technology also benefits from existing high-volume manufacturing SOI infrastructure and donor wafer recycling techniques. Compared to standard back-thinning techniques, atomic level splitting enables ultrathin (down to 0.1µm) layer transfer, simplifying the TSV process just described. With a smaller TSV aspect ratio, the Smart Cut technology is suited to high-volume applications that require higher interconnect densities.

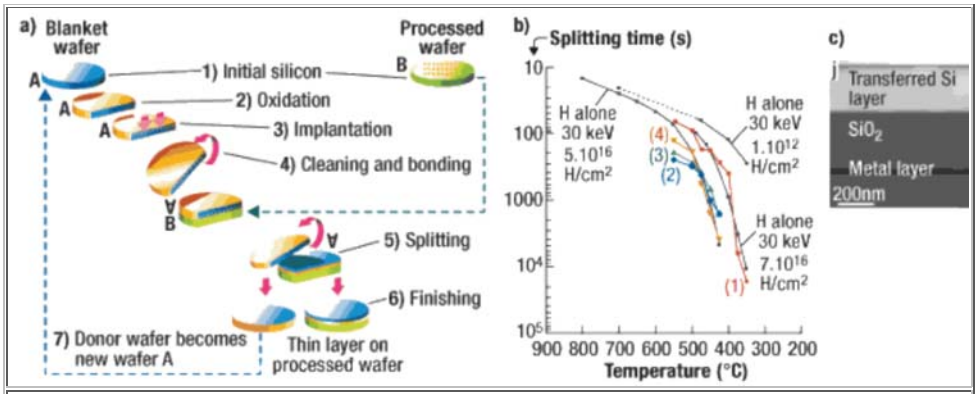


Figure 3. Process schematic of the Smart Cut Technology (a); Splitting kinetics (b); Cross-section showing a single crystalline Si layer transferred onto a wafer with a metal pattern (c).

The approach is based on Soitec's ability to optimize the bonding energy while diminishing the overall thermal budget (as done for Smart Stacking), as well as optimizing the implantation process to lower the required energy for splitting. We are able to tune the splitting kinetics and have demonstrated splitting at <350°C [9]. Preliminary defectivity inspection is promising. After splitting and surface-smoothing, wafers pass visual inspection, and show a low number of smaller defects (<120nm). The data from the early stages of development is encouraging, indicating the potential for a high-volume process.

Metal-to-metal bonding development

Immediate circuit stacking after standard backend processes is desirable as an alternative way to stack 3D IC systems. The main interest is to realize interconnections in the 3D stack during the bonding. Metal-to-metal bonding technology can be adapted with via first and via last integration schemes.

Many metal-to-metal bonding approaches have been demonstrated, including thermo compression [10,11], direct copper bonding under ultra-vacuum [12,13], and eutectic bonding (such as Cu/Sn [14]). In general, these approaches require either ultra-high vacuum, high pressure and/or high temperature. We have investigated and demonstrated a direct hydrophilic copper-to-copper bonding at room temperature, ambient air, atmospheric pressure, and without applying an external stress [15]. In contrast to the standard thermo compression bonding, this process has no additional pressure applied on the bonding stack, and lower thermal budget ensuring minimal distortion and misalignment [16]. This bonding process also does not require any additional processing steps, other than planarization and surface treatment techniques to ensure smooth hydrophilic surfaces for good bonding conditions.

At room temperature, the Cu/Cu bonding energy was recorded at 2.8J/m^2 on blanket-bonded wafers, as measured by Maszara's technique [17]. At 200°C annealing and higher, the bonding strength increases. Copper interdiffusion and/or grain growth are the driving forces for achieving high bond strength, as shown in **Fig. 4.**

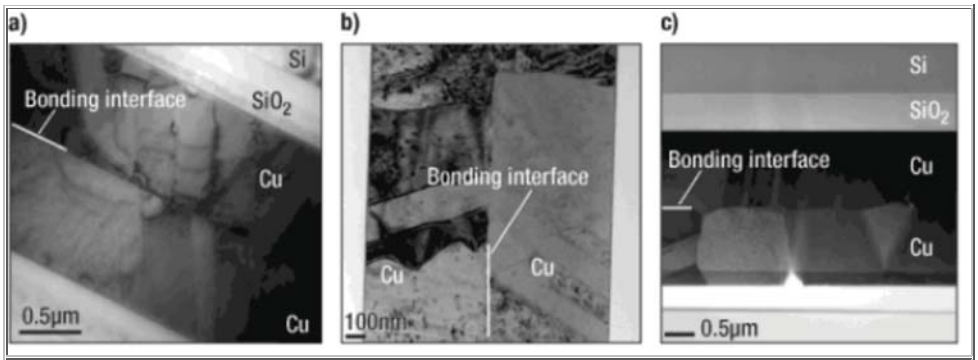


Figure 4. TEM cross-section of the bonding interface before annealing (a). Copper interdiffusion observed after 200°C (b) and 400°C annealing (c).

An electric test was conducted, highlighting the ohmic behavior of the bonding interface when the current is forced through the interface. The exhibited ohmic behavior is the outcome of optimized pre-bonding surface treatments that result in high quality Cu/Cu interface. Furthermore, ohmic resistance was measured by a 4-point probe showing specific contact resistance $\rho c = 0.98\Omega.\mu m^2$ on a $10\times10\mu m^2$ contact area after annealing at 200°C for 30 minutes [18].

In addition, wafer-to-wafer alignment capability of $<\pm1\mu m$ has been demonstrated without distortion of the wafers [19]. The copper-to-copper non-thermo compression bonding has other advantages that contribute to a loweroverall process cost of ownership, including a faster cycle time compared to thermo compression bonding [16].

Conclusion

We have presented technologies that are candidate building blocks for different 3D integration schemes. We demonstrated the compatibility of these building blocks with back-end-of- line CMOS processes and with aggressive wafer grinding and thinning. The Smart Stacking technology and copper-to-copper non-thermo compression bonding processes were described as key technologies to realize dielectric or metallic bonding at room temperature and without applied pressure and/or a glue layer. The Smart Cut technology was presented as an option that provides a new surface on which new devices can be processed, and also as an integration scheme well-suited for applications that require higher interconnect densities. Based on these promising technologies, the 3D building blocks fulfill therequirements for wafer-level 3D integration schemes.

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Mariam Sadaka received her PhD in chemical engineering from Arizona State U. and an MBA from The U. of Texas at Austin. She is a fellow leading the 3D integration team at *Soitec, 1010 Land Creek Cv, Austin, TX 78746 USA;* msadaka@soitecusa.com

Lea Di Cioccio received a PhD in material and semiconductor physics from the Institut National Polytechnique de Grenoble, France. She is a research engineer, specializing in semiconductor heterostructures and 3D integration, using various processes such as epitaxy, wafer

bonding, and thinning, at *CEA-Leti, 17 Rue des Martyrs, 38054 Grenoble, France;* lea.dicioccio@cea.fr

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