3D-IC Integration

- Developments
- Cooperation for servicing and MPW runs offering

Agenda

- Introduction
- Process overview
- Partnership for MPW runs service
- 3D-IC Design Platform
- First MPW run
- Conclusion

3D-IC Integration : Not a New Story

Akasaka, Y., and Nishimura, T., "Concept and Basic Technologies for 3-D IC Structure“
IEEE Proceedings of International Electron Devices Meetings, Vo. 32, 1986, pp. 488-491.

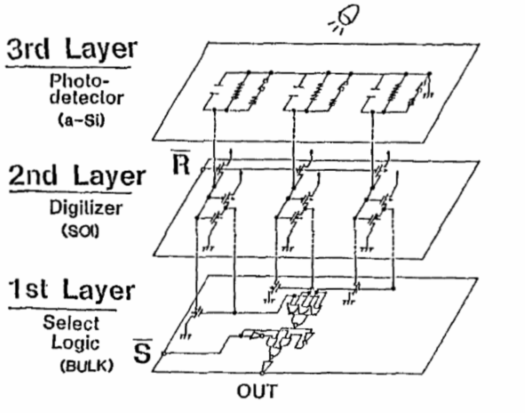


Fig.8 a-Si photo sensor and processing circuits in 3-staked layers (after Mihashi)

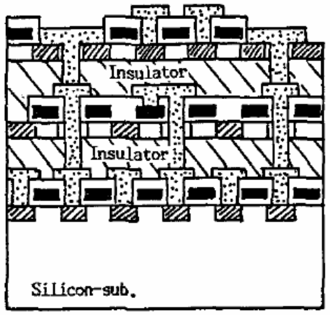


Fig.1 Schematic drawing of 3-D IC consisting of monolithic multi-layer structure.

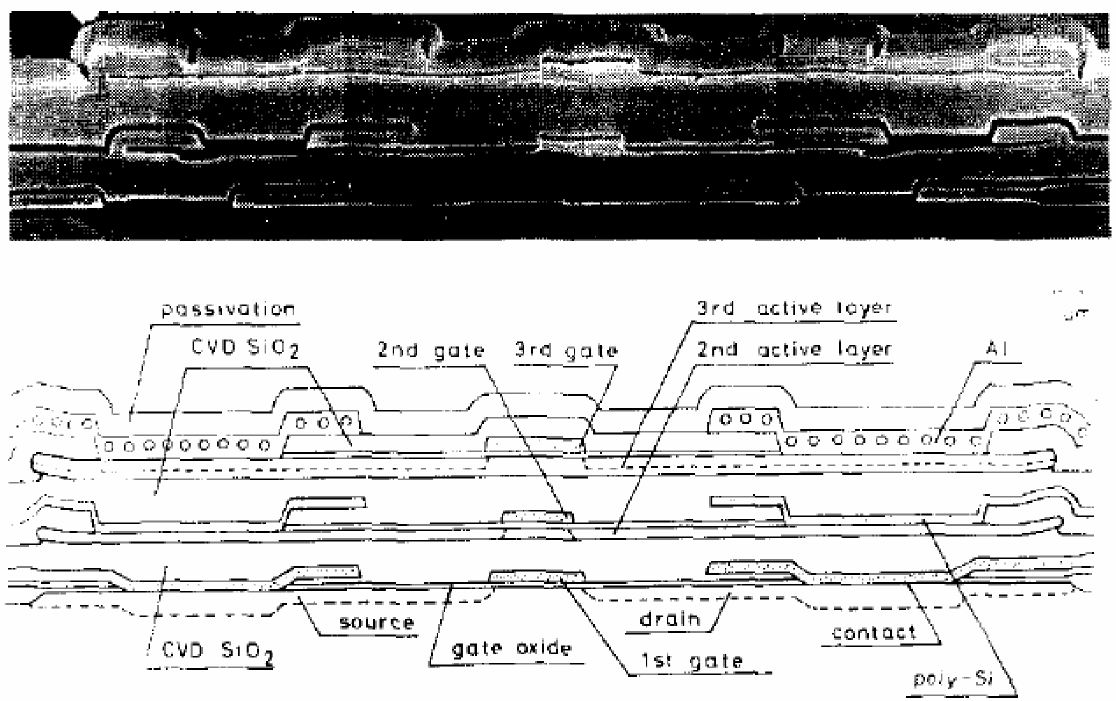
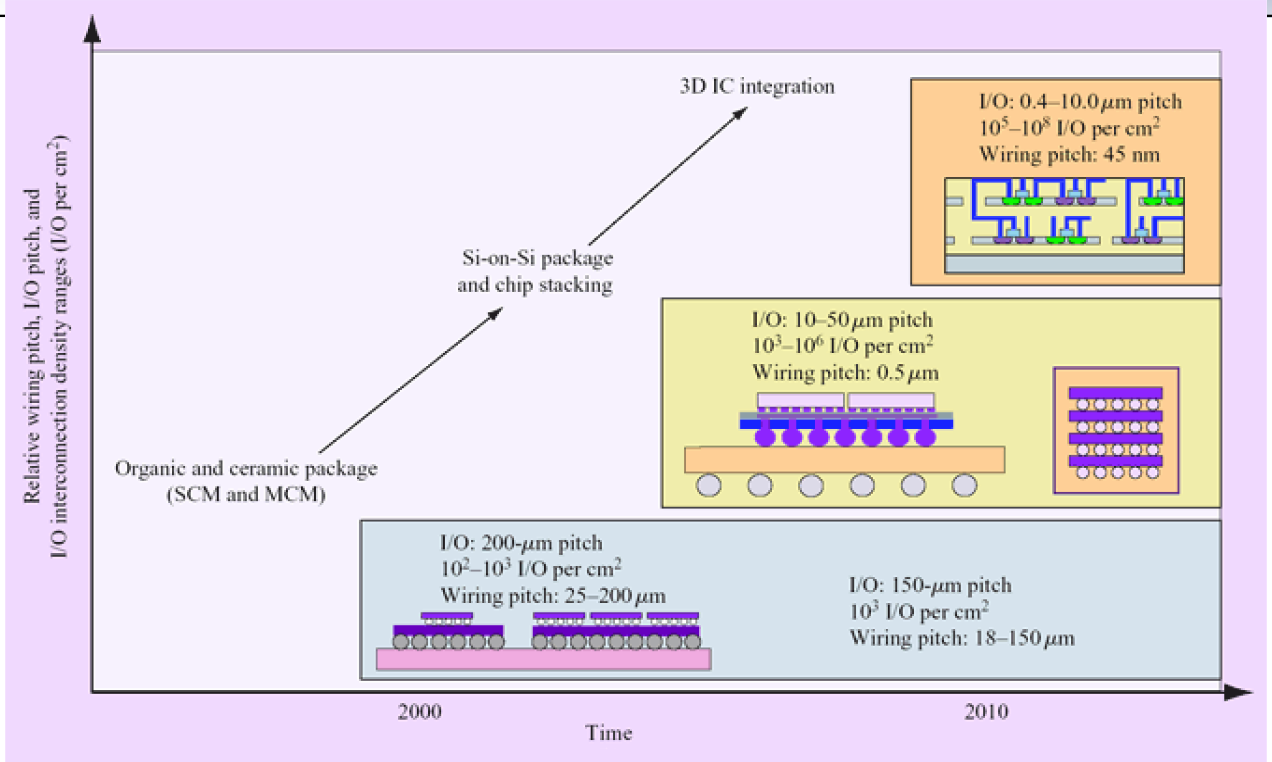


Fig.4 SEM cross sectional photograph and schematic drawing of planarized tripply-stacked IC structure.

3D-IC Integration : The Other Path for Scaling



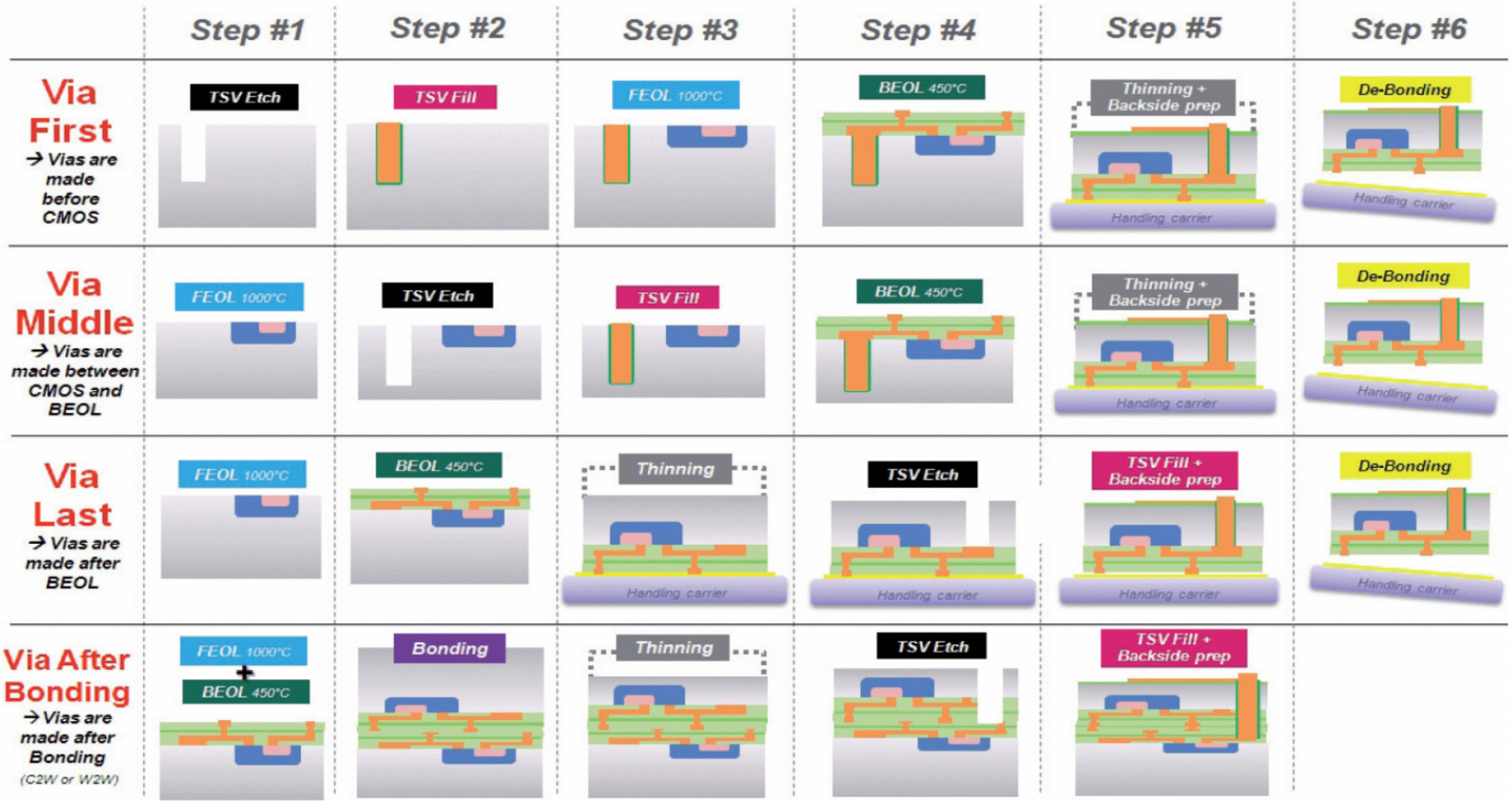
Source IBM http://www.research.ibm.com/journal/rd/526/knickerbocker.html

- **Moore’s law by scaling conventional CMOS involves huge investments.**

- **3D IC processes : An opportunity for another path towards continuing the scaling, involving less investments.**

- **Like for conventional CMOS, infrastructures are needed to promote 3D-IC integration, making it available for prototyping at “reasonable” costs.**

3D TSV via integration MAIN scenarios



	Step #1	Step #2	Step #3	Step #4	Step #5	Step #6
Via First → Vias are made before CMOS	TSV Etch	TSV Fill	FEOL 1000°C	BEOL 450°C	Thinning + Backside prep	De-Bonding
Via Middle → Vias are made between CMOS and BEOL	FEOL 1000°C	TSV Etch	TSV Fill	BEOL 450°C	Thinning + Backside prep	De-Bonding
Via Last → Vias are made after BEOL	FEOL 1000°C	BEOL 450°C	Thinning	TSV Etch	TSV Fill + Backside prep	De-Bonding
Via After Bonding → Vias are made after Bonding (C2W or W2W)	FEOL 1000°C + BEOL 450°C	Bonding	Thinning	TSV Etch	TSV Fill + Backside prep	

Source Yole Development

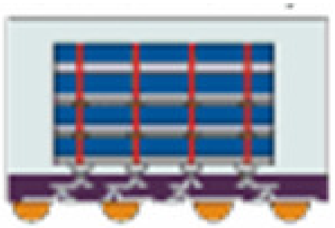
Interconnection

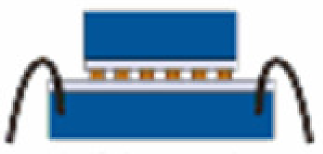
Interconnection Type	**Line Width (µm)**	**Line Thickness (µm)**	**Line Resistance (Ohm/cm)**	**Max Length (cm)**
Direct Bond Interface (DBI)	2-100	2-100	0	0
Through Si Via (TSV)	1-100	1-100	500-1000	5-100
On-Chip	0.1-2	0.1-2	100-1000	0.1-1.5
Thin-film	10-25	5-8	1.25-4	20-45
Ceramic	75-100	16-25	0.4-0.7	20-50
Printed Circuit Board	60-100	30-50	0.06-0.08	40-70
Shielded Cables	100-450	35-450	0.0013-0.033	150-500

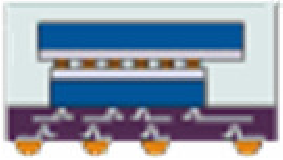
Different Integration Approaches

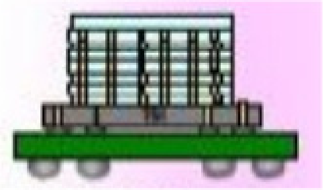
“Monolithic”

Distributing a whole system across several tiers

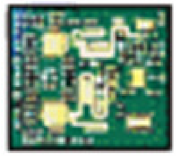

3D-IC TSV Stacked Memory


3D-IC face to face


3D-IC TSV integrated

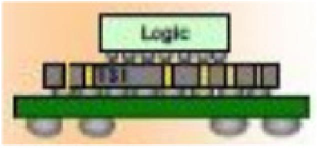

Heterogeneous Multi layer
3D-IC TSV integrated

Integration


Substrate based
Module (PCB)


Multi-Chip Module


Die to Die Integrated package



Silicon Interposer to high
Integrated MCM

“Discrete”

Assembly of “Known Good Dies”

Which Design Methodology ?

- Discrete : 3D packaging, stacked dies, …

  1- Design a whole system.
  2- Split it in subsystems.
  3- Place the subsystems as predefined “Known Good Dies” (IPs).
  4- Determine and place the interfaces in between.
  5- The system is done

- Monolithic : 3D-IC Integration

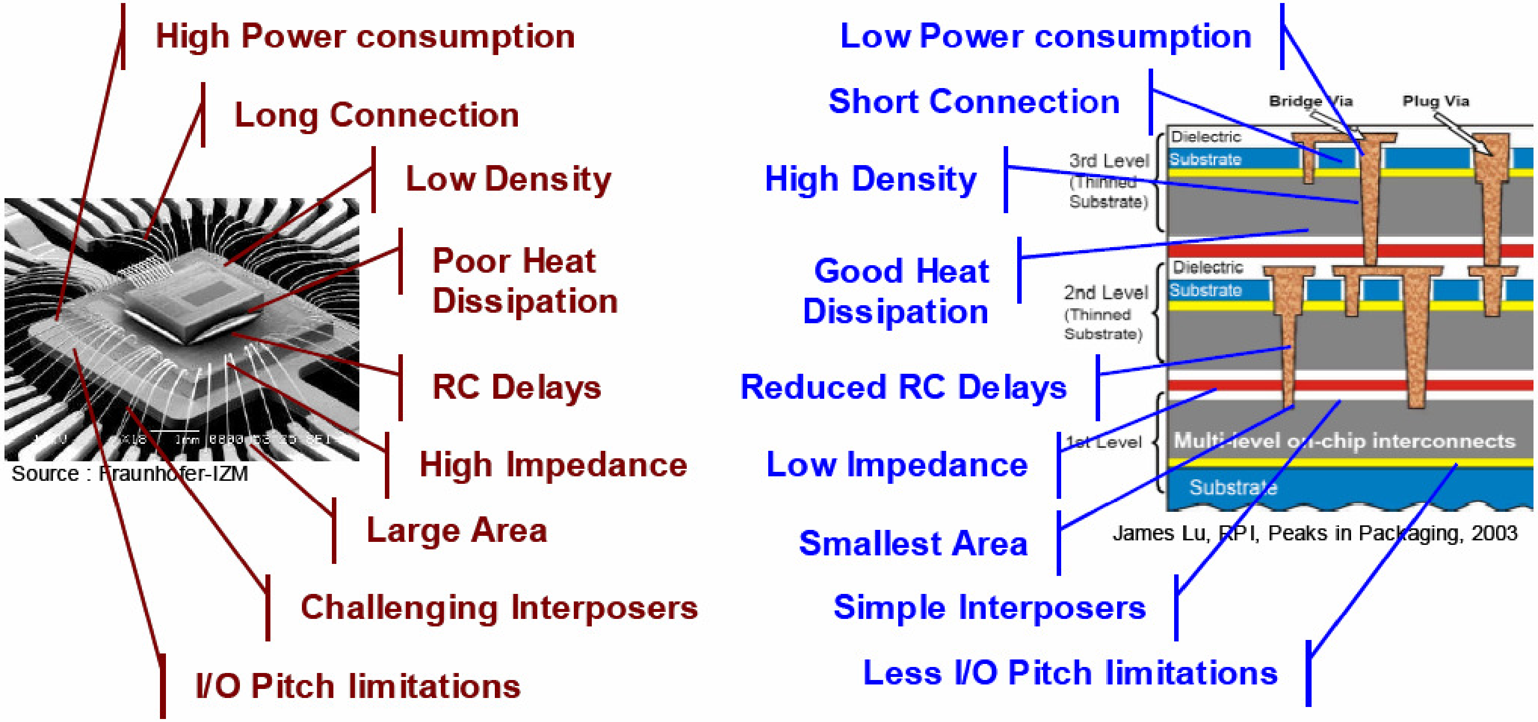
  1- Design a whole system.
  2- Split it in subsystems.
  3- Determine and place the interfaces in between.
  4- Generate and Place the subsystems in between the interfaces.
  5- The system is done

Here comes the difference : The “key” for a true 3D-IC Integration

SiP versus 3D-IC

Why TSV Interconnection?

TSV (Through-Silicon-Via) electrodes can provide vertical connections that are both the shortest and the most plentiful.



Source : Fraunhofer-IZM

James Lu, RPI, Peaks in Packaging, 2003

High Power consumption	**Low Power consumption**
Long Connection	**Short Connection**
Low Density	**High Density**
Poor Heat Dissipation	**Good Heat Dissipation**
RC Delays	**Reduced RC Delays**
High Impedance	**Low Impedance**
Large Area	**Smallest Area**
Challenging Interposers	**Simple Interposers**
I/O Pitch limitations	**Less I/O Pitch limitations**

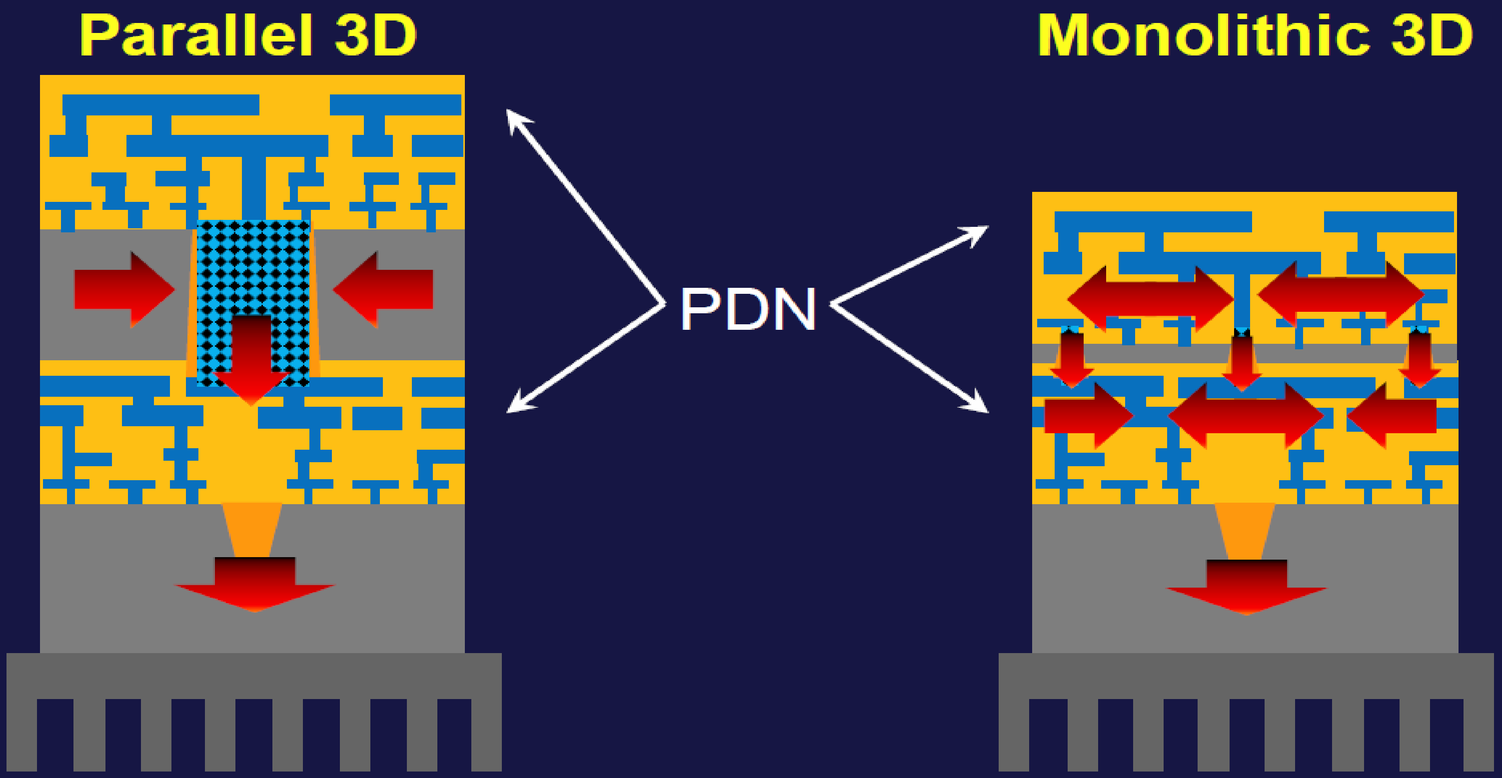
TSV interconnects provide solutions to many limitations of current SiP and Chip Stacking methods.

Ecole Polytechnique Paris - 3D Technical Symposium; November 2007

Page3

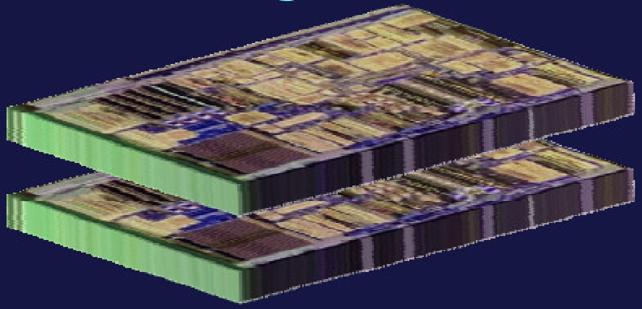
Geometries

- PDN: Power Delivery Network



Cooling Three-Dimensional Integrated Circuits using Power Delivery Networks
Hai Wei*+, Tony F. Wu+, Deepak Sekar&, Brian Cronquist#, Roger Fabian Pease+, Subhasish Mitra+^
Department of Electrical Engineering+ and Department of Computer Science^, Stanford University, Stanford, CA,
Monolithic 3D Inc.#, San Jose, CA, Rambus&, Sunnyvale, CA, Email*: haiwei@stanford.edu

Key Result for Monolithic 3D



OpenSPARC T2 core-on-core

Cooling Three-Dimensional Integrated Circuits using Power Delivery Networks

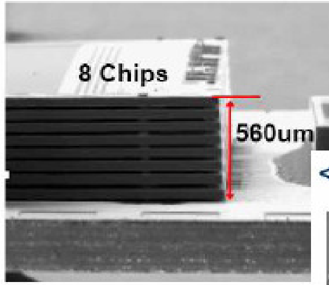
Hai Wei*+, Tony F. Wu+, Deepak Sekar&, Brian Cronquist#, Roger Fabian Pease+, Subhasish Mitra+^
Department of Electrical Engineering+ and Department of Computer Science^, Stanford University, Stanford, CA,
Monolithic 3D Inc.#, San Jose, CA, Rambus&, Sunnyvale, CA, Email*: haiwei@stanford.edu

3D-IC Applications

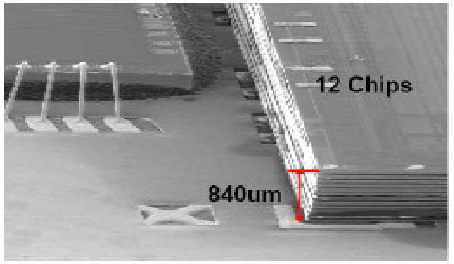
Industrial Applications

- There are two 3D areas that are receiving a lot of attention.
  - Stacked memory chips and memory on CPU
    - IBM expected to provide samples later this year
    - Both IBM and Samsung could be in production next year (2008)
  - Imaging arrays (pixelated devices)
    - Working devices have been demonstrated by MIT LL, RTI, and Ziptronix
    - Much work is supported by DARPA
- Pixel arrays offer the most promise for HEP projects.

< NAND 8 Stacked Memory Card >

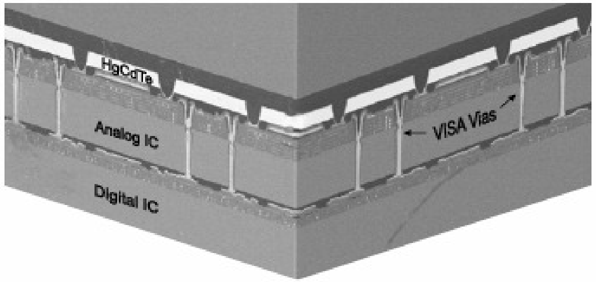


< NAND 12 Stacked Memory Card >



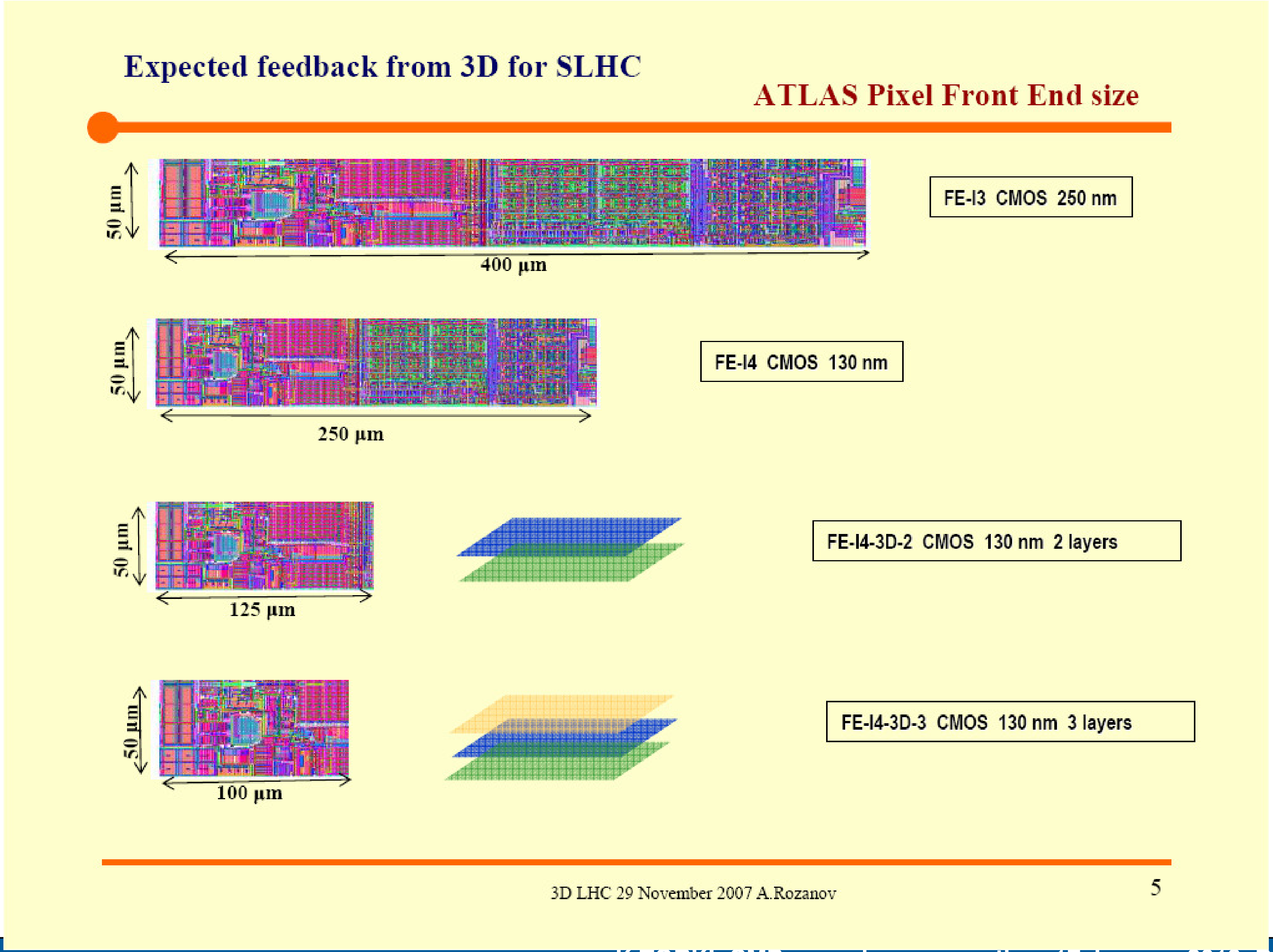
Samsung - 30 um laser drilled vias in 70um chips

RTI Infrared Imager



LHC-ILC Workshop on 3D Integration Techniques

3D Microelectronics for Physics (FermiLab, IN2P3, INFN, CERN)



Expected feedback from 3D for SLHC

ATLAS Pixel Front End size

FE-I3 CMOS 250 nm

FE-I4 CMOS 130 nm

FE-I4-3D-2 CMOS 130 nm 2 layers

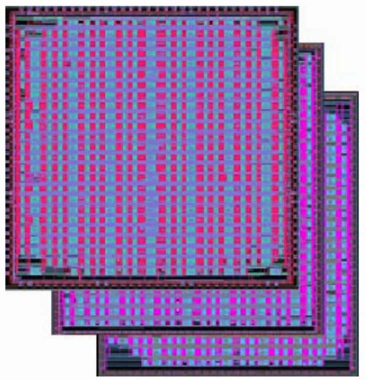
FE-I4-3D-3 CMOS 130 nm 3 layers

3D LHC 29 November 2007 A.Rozanov

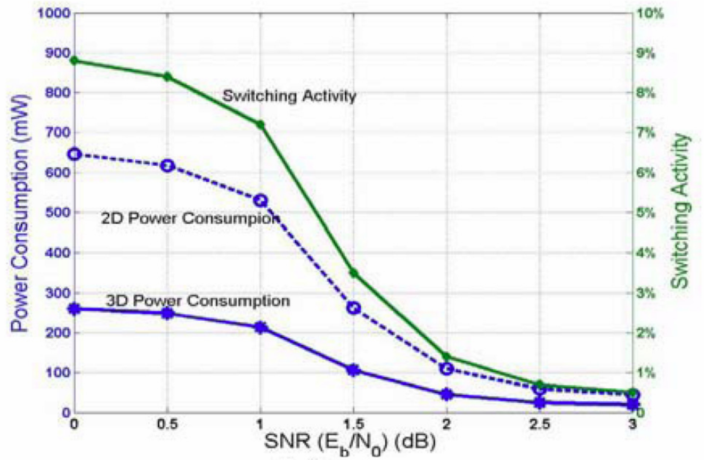
5

Large Systems Benefits from 3D-IC Integration

"Implementing a 2-Gbs 1024-bit ½-rate Low-Density Parity-Check Code Decoder in Three-Dimensional Integrated Circuits"
Lili Zhou, Cherry Wakayama, Robin Panda, Nuttorn Jangkrajarng, Bo Hu, and C.-J. Richard Shi
University of Washington
International Conference on Computer Design, ICCD, Oct. 2007

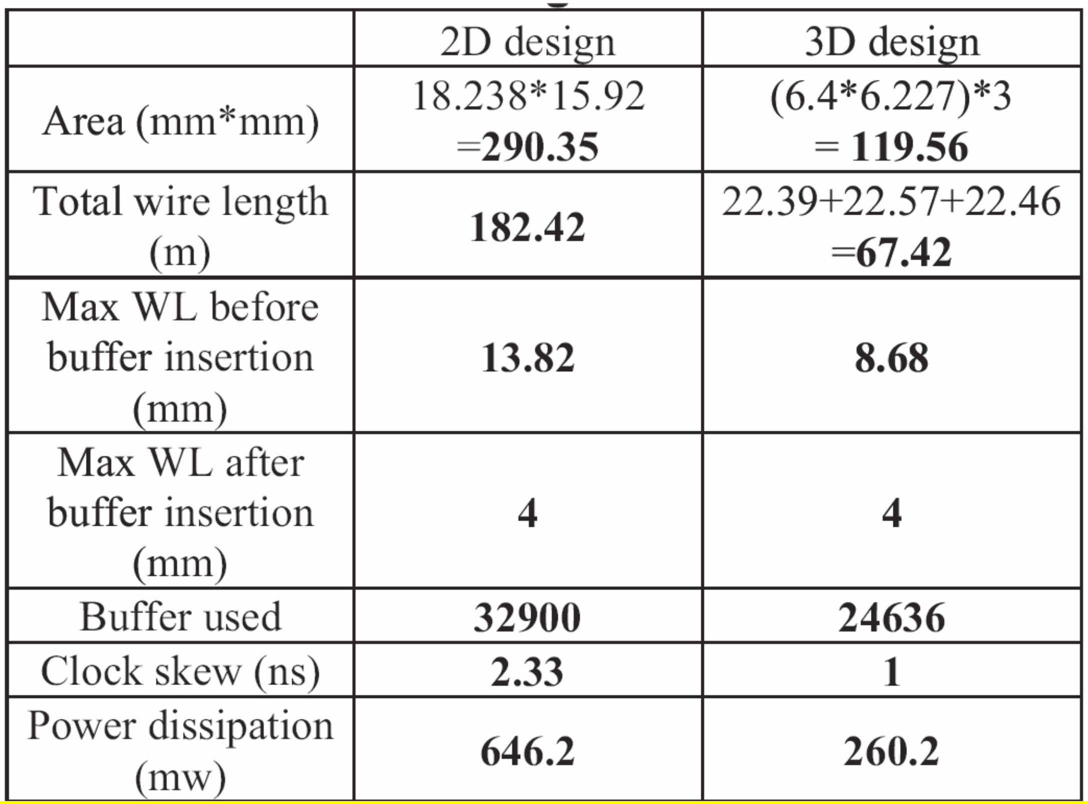


Final layout view of 3D LDPC structure.



Post-layout power of the LDPC decoder (2D vs 3D).

Comparison between 3D and 2D designs

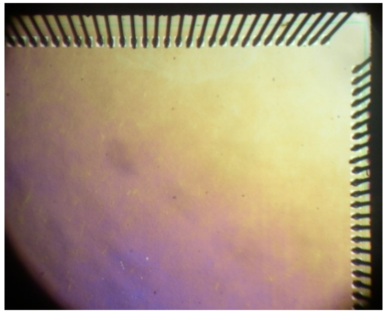


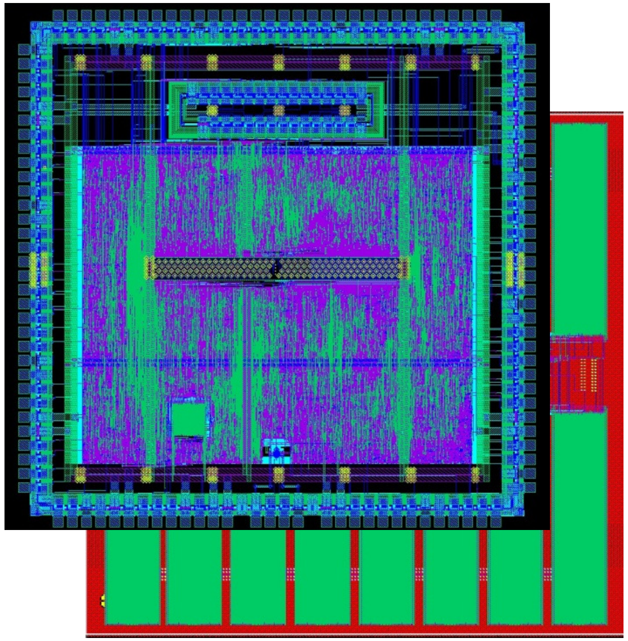
	2D design	3D design
Area (mm*mm)	18.238*15.92 =**290.35**	(6.4*6.227)*3 = **119.56**
Total wire length (m)	**182.42**	22.39+22.57+22.46 =**67.42**
Max WL before buffer insertion (mm)	**13.82**	**8.68**
Max WL after buffer insertion (mm)	**4**	**4**
Buffer used	**32900**	**24636**
Clock skew (ns)	**2.33**	**1**
Power dissipation (mw)	**646.2**	**260.2**

Performance Factor (Area * Timing * Power) = 14

An Illustration: CPU/Memory Stack

- R8051 CPU
  - 80MHz operation; 140MHz Lab test (VDD High)
  - 220MHz Memory interface
- IEEE 754 Floating point coprocessor
- 32 bit Integer coprocessor
- 2 UARTs, Int. Cont., 3 Timers, …
- Crypto functions
- 128KBytes/layer main memory





- 5X performance
- 1/10th Power

Source Tezzaron (2004)

Some 3D-IC Applications

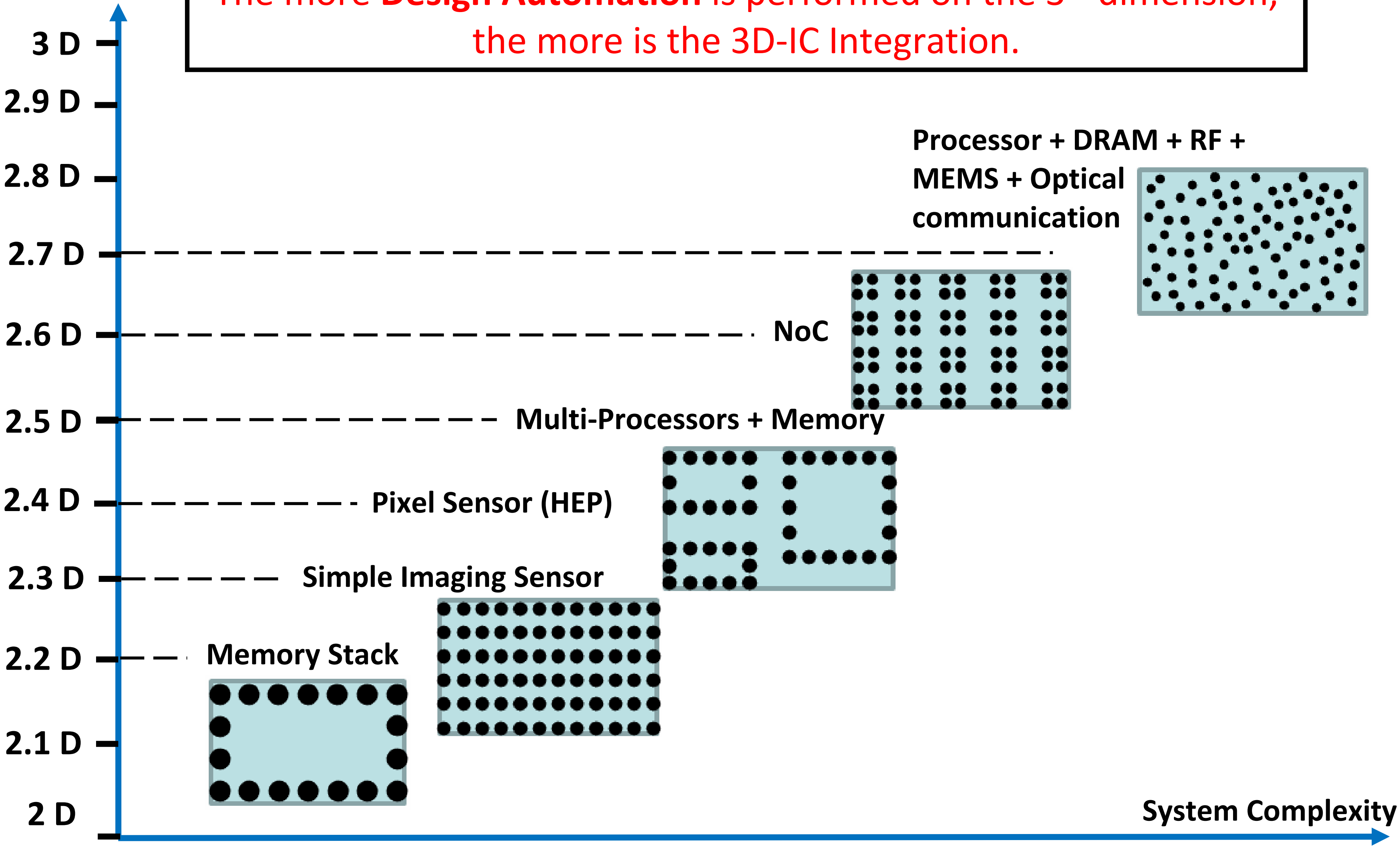
- Pixel array for Particle detection (HEP community)

(Pixel sensor + Analog + Digital + Memory + high speed I/Os)

- CMOS Image Sensor (Sensor + Processor + Memory)
- 3D stacked Memories (Flash, DRAM, etc…)
- Multi-cores Processor + Cache Memory
- NoC (Network on Chip)
- Processor + DRAM + RF + MEMS + Optical communication + …

Design Methodology

The more **Design Automation** is performed on the 3rd dimension, the more is the 3D-IC Integration.



CMC-CMP-MOSIS Collaboration

CMC / CMP / MOSIS partnering for 3D-IC process access

- Stimulate the activity by sharing the expenses for manufacturing.
- Join forces for the technical support, and dedicate the roles for each partner.
- Make easier the tech support for local users respectively by each local center.
- Because there is no standard for the 3D-IC integration, it is urgent to setup an infrastructure making possible a broad adoption of 3D-ICs. That will have a beneficial effect on prices, more frequent MPW runs, and more skilled engineers.

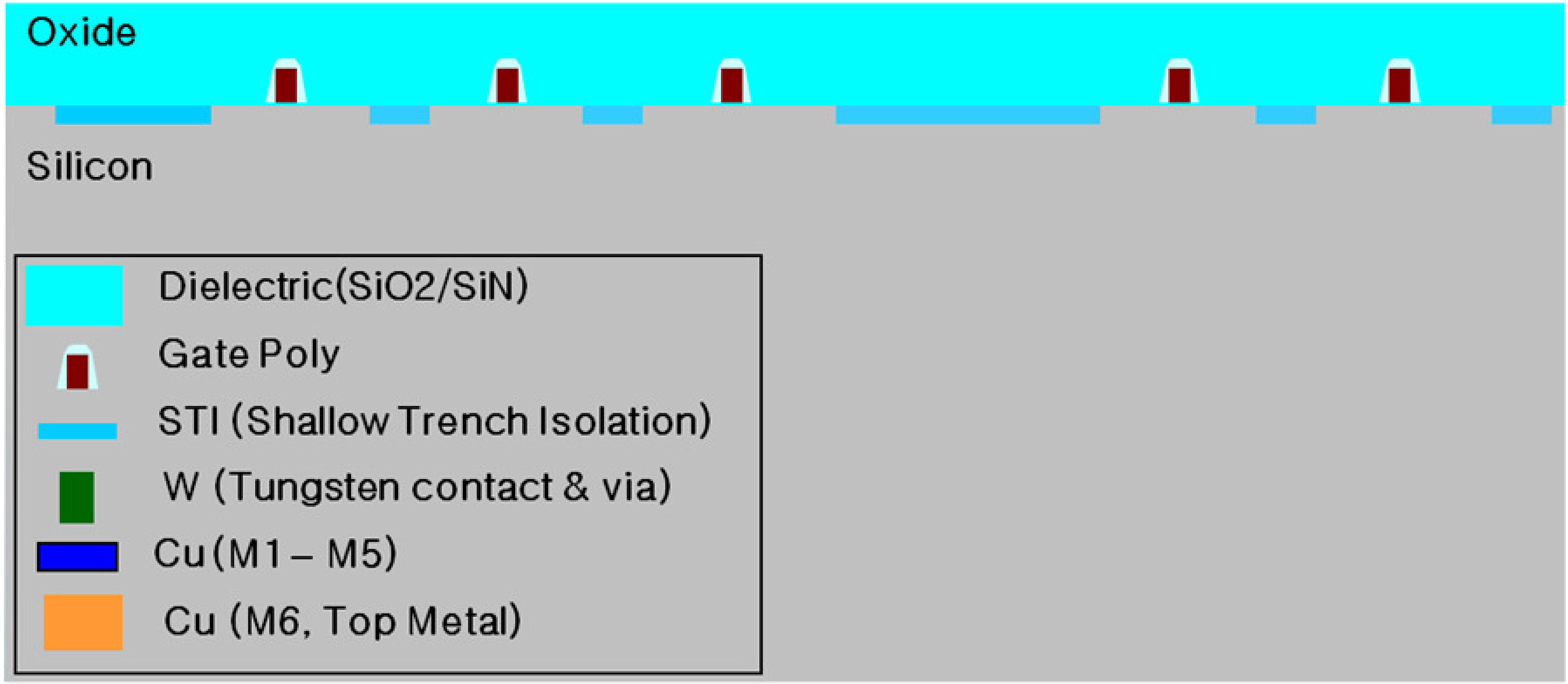
CMC - CMP - MOSIS Cooperation

- CMC supporting Canadian Customers
- CMP supporting European Customers
- MOSIS supporting US Customers
- Each may support other locations

Tezzaron 2-Tier Process (130nm CMOS)

Process Overview

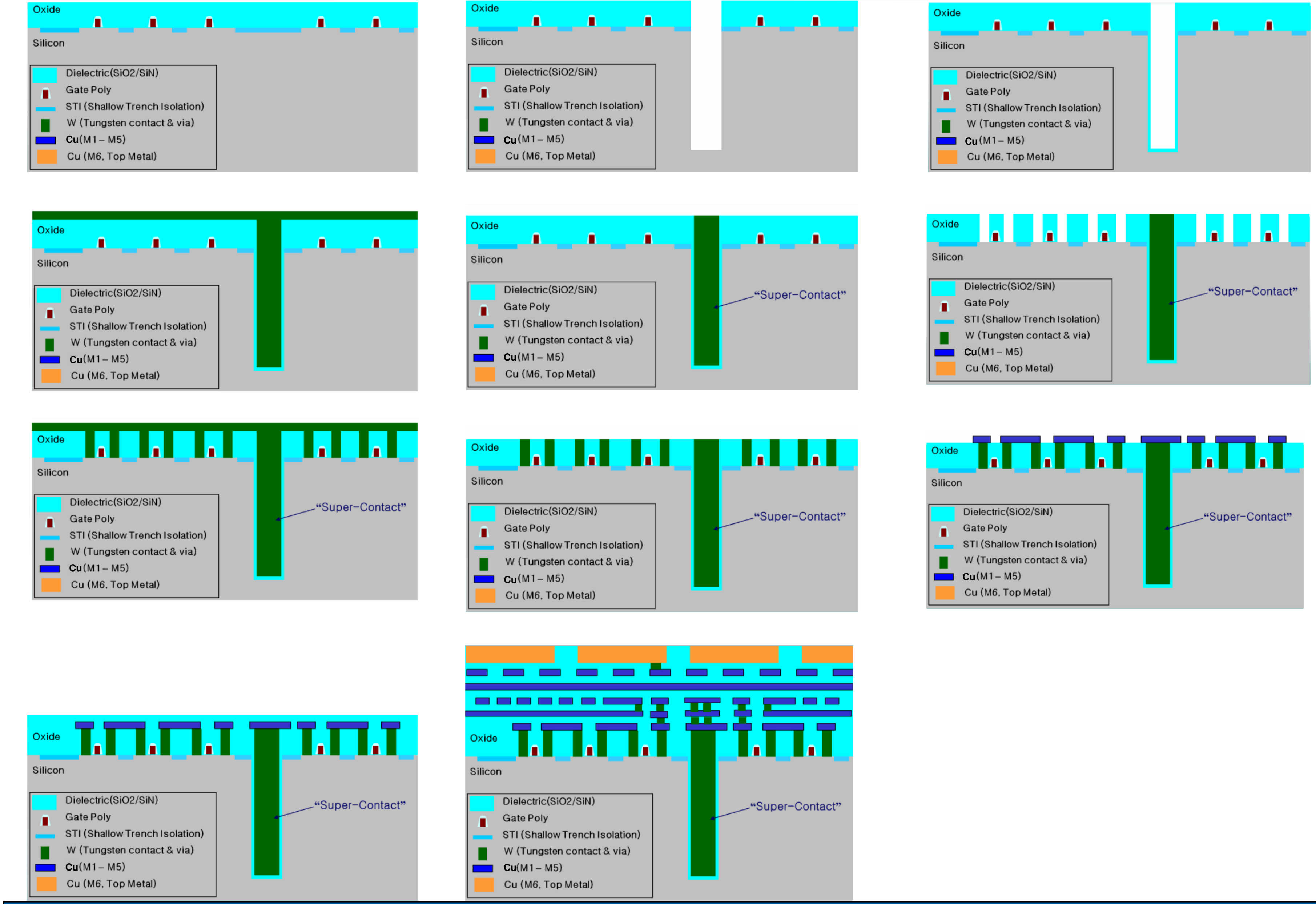
Tezzaron Process Flow for TSV and DBI (using Via Middle process)



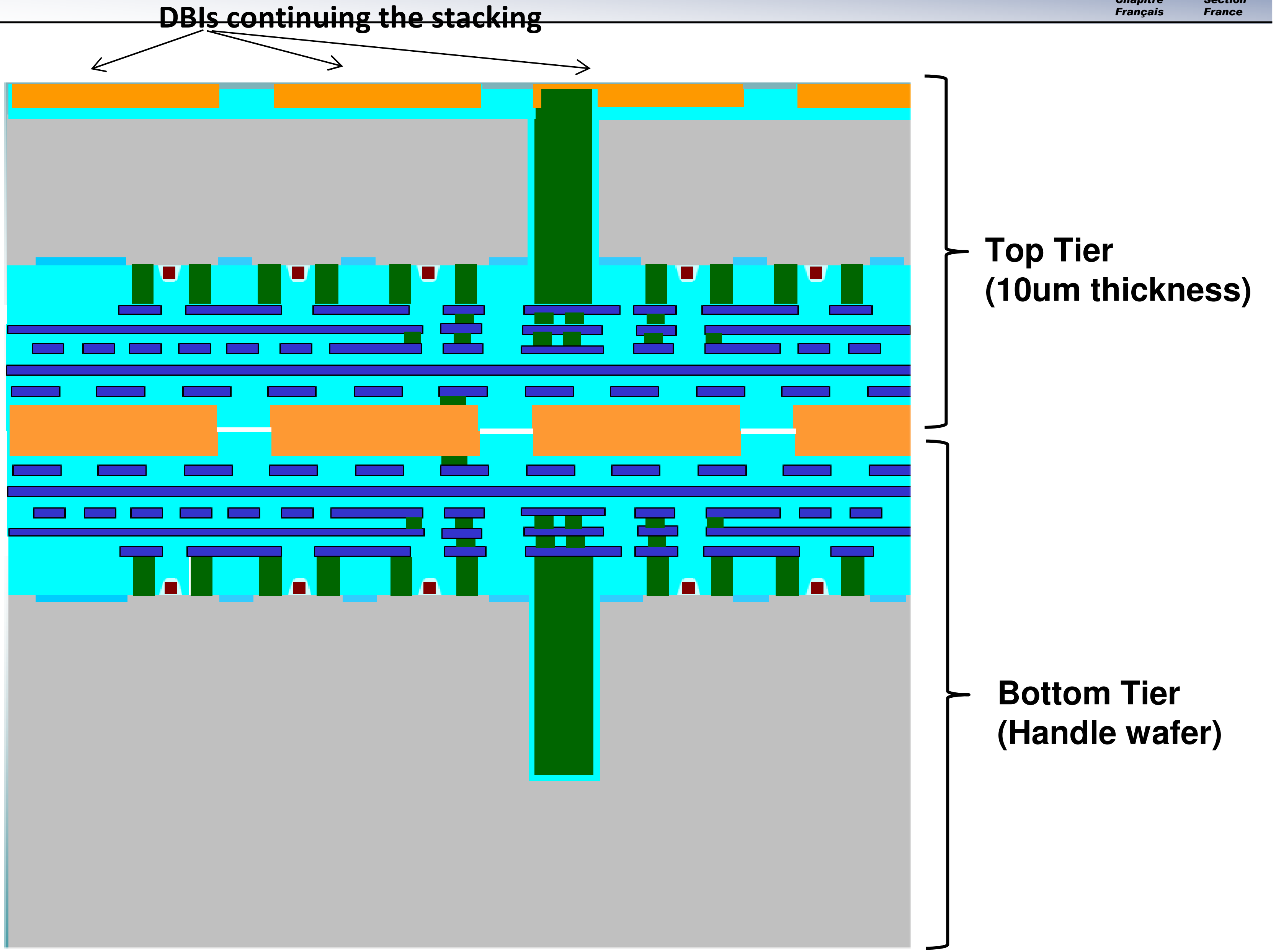
Starting wafer in 130nm (5 Cu metal layers + 6th Cu metal as DBI)

Source Tezzaron

Tezzaron Process Flow for TSV and DBI (using Via Middle process)

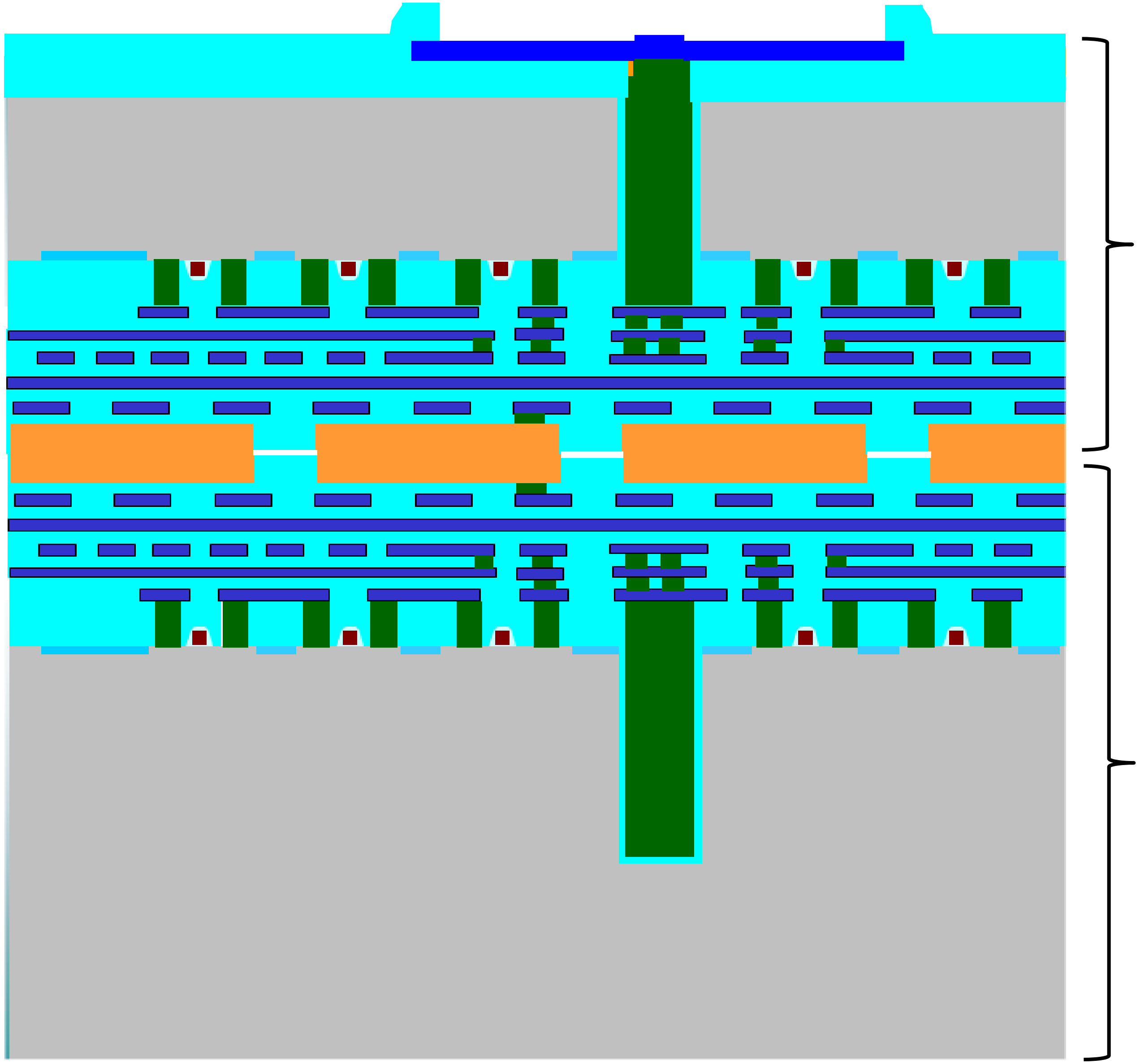


Resulting 2-tier 3D-IC integration TSV and DBI (Via Middle Process)



Source Tezzaron

Resulting 2-tier 3D-IC integration TSV and DBI (Via Middle Process)


Bond pad for wire bonding or bump, flip-chip …

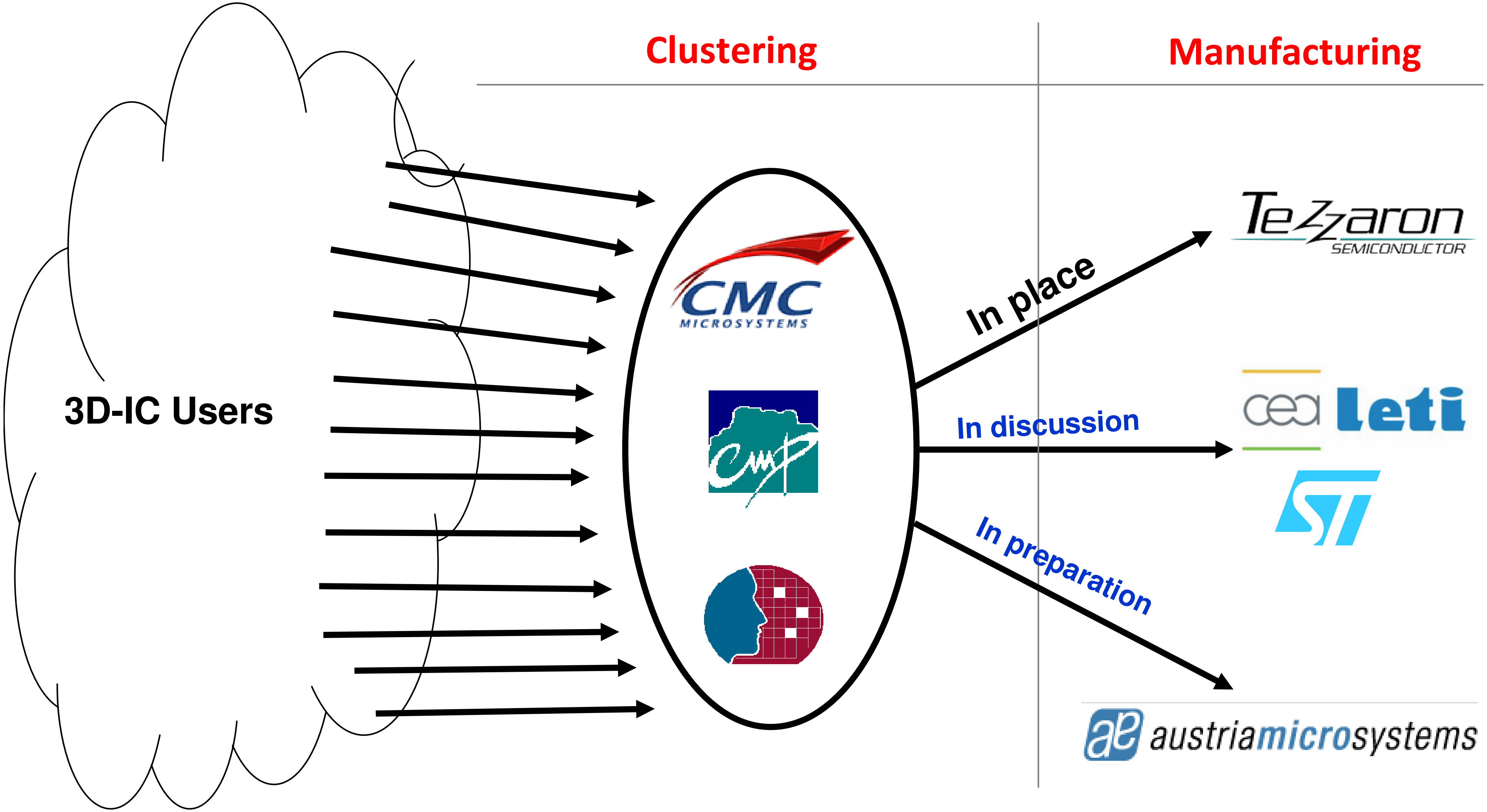
Top Tier (10um thickness)

Bottom Tier (Handle wafer)

Source Tezzaron

3D-IC MPW Infrastructure

CMC-CMP-MOSIS partnering to offer 3D-IC MPW runs



Clustering

Manufacturing

3D-IC Users

In place

In discussion

In preparation

Critical mass will allow frequent MPW runs and low pricing

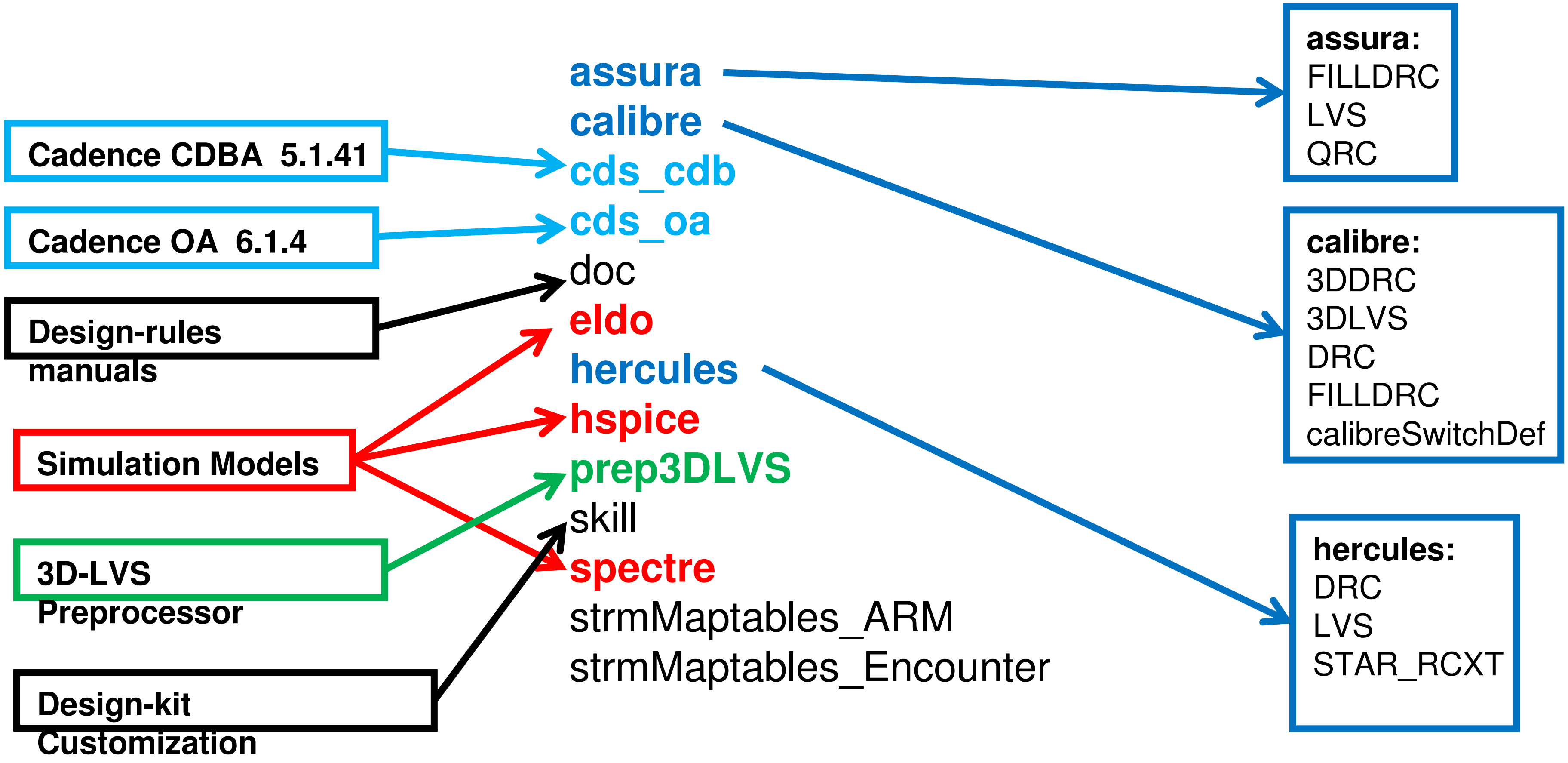
3D-IC Design Platform

Tezzaron / GlobalFoundries Design Platform

- The Design Platform is modular. It has all features for full-custom design or semi-custom automatic generation design.
  - **PDK :** ***Original PDK from GF + (TSV / DBI) definition from Tezzaron***
  - **Libraries :** ***CORE and IO standard libraries from ARM***
  - **Memory compilers :** ***SPRAM, DPRAM and ROM from ARM***
  - **3D-IC Utilities :** ***Contributions developments embedded in the platform***
  - **Tutorials, User's setup.**
- All modules inside the platform refer to a unique variable, making it portable to any site. The installation procedure is straightforward.
- Support of CDBA and OpenAccess databases.

PDK Tezzaron / GlobalFoundries

chrt13lprf_DK009_Rev_1D (Version issued in Q2 2011)



Cadence CDBA 5.1.41

Cadence OA 6.1.4

Design-rules manuals

Simulation Models

3D-LVS Preprocessor

Design-kit Customization

assura
calibre
cds_cdb
cds_oa
doc
eldo
hercules
hspice
prep3DLVS
skill
spectre
strmMaptables_ARM
strmMaptables_Encounter

assura:
FILLDRC
LVS
QRC

calibre:
3DDRC
3DLVS
DRC
FILLDRC
calibreSwitchDef

hercules:
DRC
LVS
STAR_RCXT

Collaborative Work to the Design Platform

HEP labs contributing with Programs, Libraries, and Utilities. All included in the Design Platform

- DBI (direct bonding interface) cells library. (FermiLab)
- 3D Pad template compatible with the ARM IO lib. (IPHC)
- Preprocessor for 3D LVS / Calibre (NCSU)
- Skill program to generate an array of labels (IPHC)
- Calibre 3D DRC (Univ. of Bonn)
- Dummies filling generator under Assura (CMP)
- Basic logic cells and IO pads (FermiLab)
- Floor-planning / automatic Place & Route using DBIs, and TSVs (CMP)
- Skill program generating automatically sealrings and scribes (FermiLab)
- MicroMagic PDK (Tezzaron/NCSU)

Virtuoso Layout Editor with 3D layers and verification

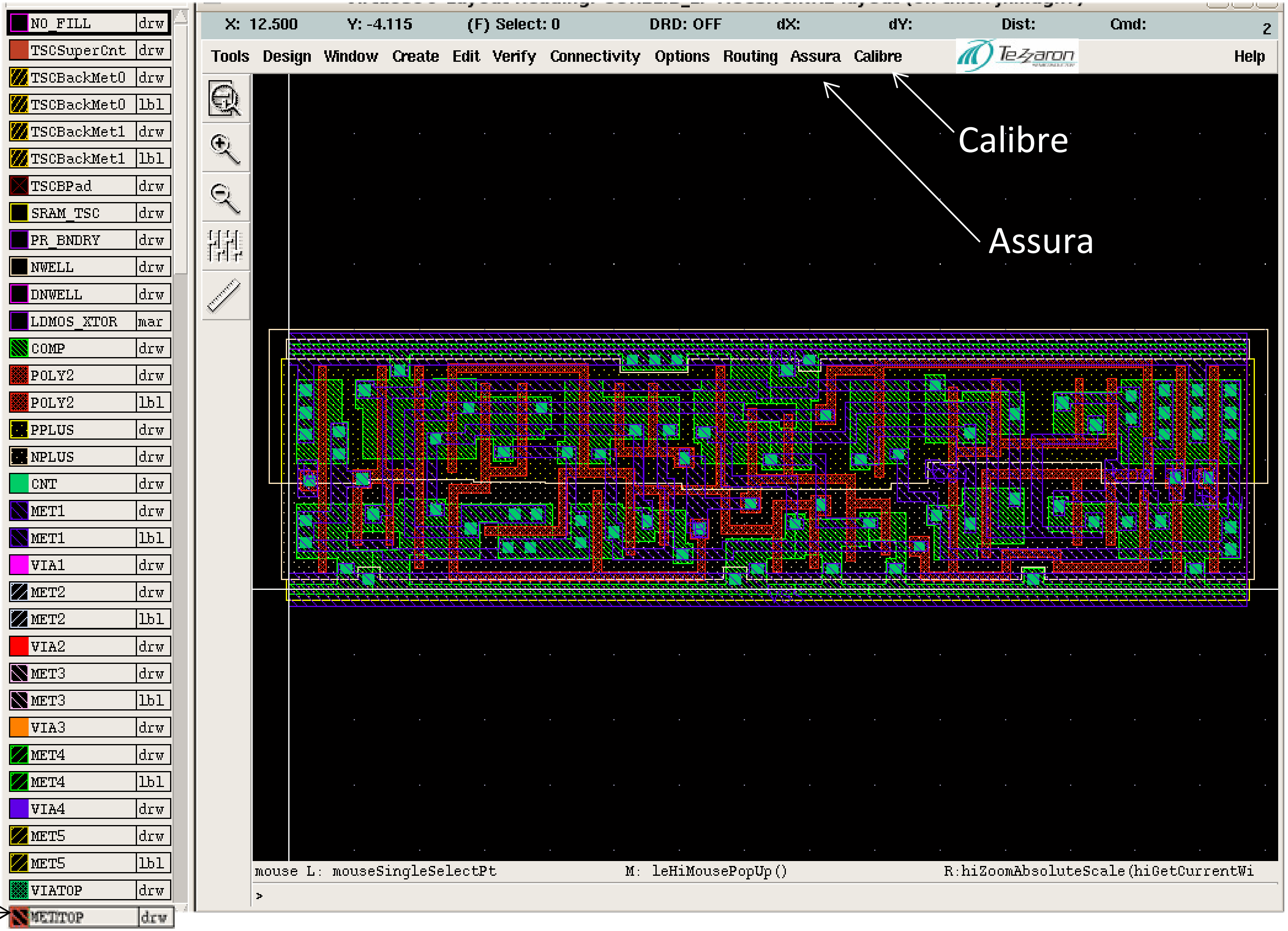
Virtuoso / Cadence IC 5.1.41

TSV

Back Metal

Back Pad

DBI



```
X: 12.500    Y: -4.115    (F) Select: 0    DRD: OFF    dX:    dY:    Dist:    Cmd:    2
```

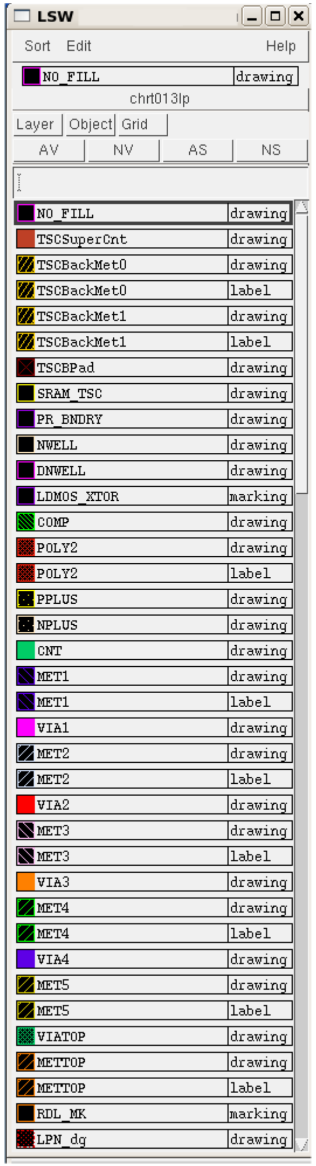
```
mouse L: mouseSingleSelectPt          M: leHiMousePopUp()          R:hiZoomAbsoluteScale(hiGetCurrentWi
>
```

Calibre

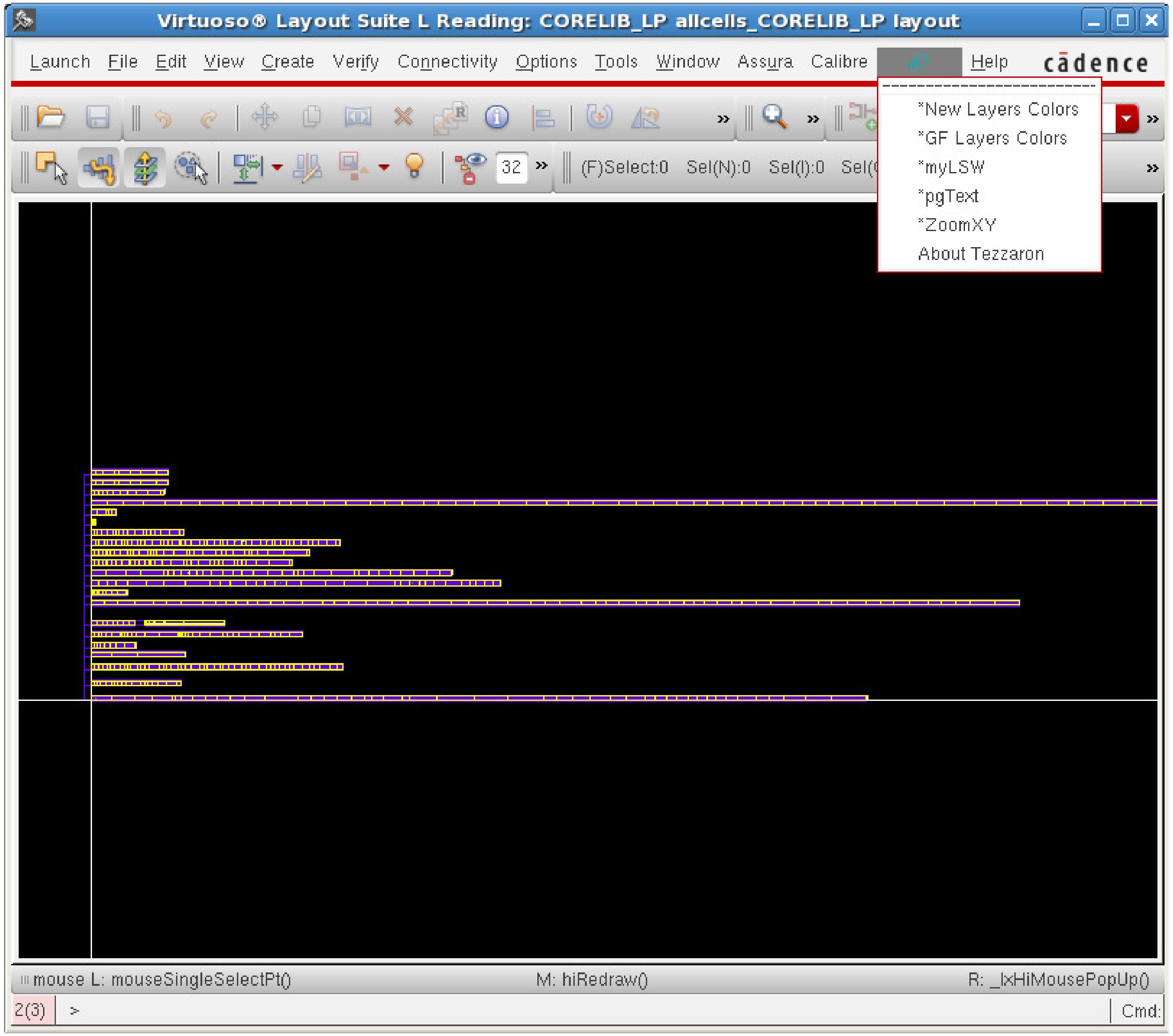
Assura

Customized Menu with some utilities

Virtuoso / Cadence IC 6.1.4

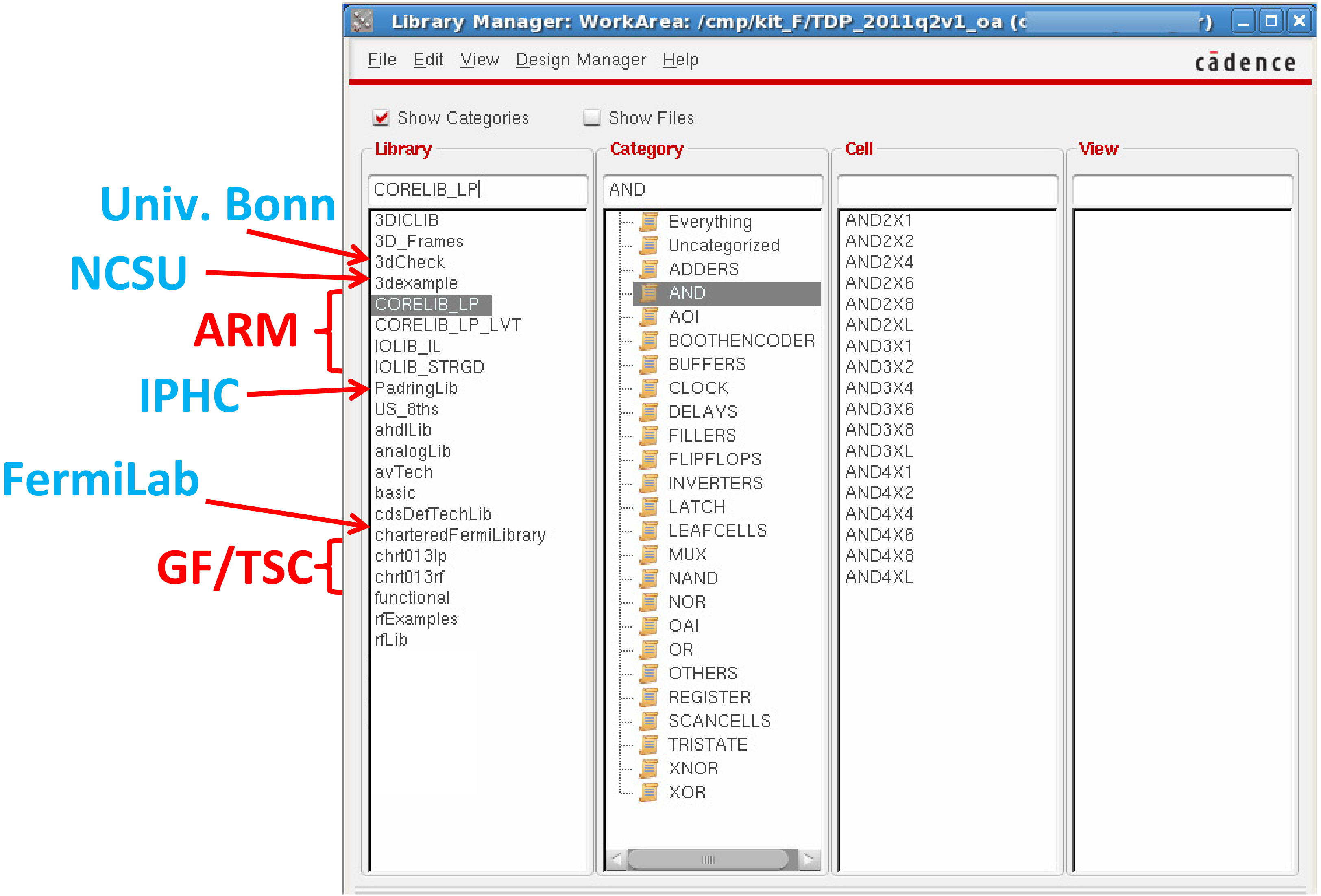


NO_FILL	drawing
TSCSuperCnt	drawing
TSCBackMet0	drawing
TSCBackMet0	label
TSCBackMet1	drawing
TSCBackMet1	label
TSCBPad	drawing
SRAM_TSC	drawing
PR_BNDRY	drawing
NWELL	drawing
DNWELL	drawing
LDMOS_XTOR	marking
COMP	drawing
POLY2	drawing
POLY2	label
PPLUS	drawing
NPLUS	drawing
CNT	drawing
MET1	drawing
MET1	label
VIA1	drawing
MET2	drawing
MET2	label
VIA2	drawing
MET3	drawing
MET3	label
VIA3	drawing
MET4	drawing
MET4	label
VIA4	drawing
MET5	drawing
MET5	label
VIATOP	drawing
METTOP	drawing
METTOP	label
RDL_MK	marking
LPN_dg	drawing


Virtuoso® Layout Suite L Reading: CORELIB_LP allcells_CORELIB_LP layout

mouse L: mouseSingleSelectPt()
M: hiRedraw()
R: _lxHiMousePopUp()
Cmd:

Libraries from Providers and Users



Univ. Bonn

NCSU

ARM

IPHC

FermiLab

GF/TSC

☑ Show Categories ☐ Show Files

Library: CORELIB_LP

- 3DICLIB
- 3D_Frames
- 3dCheck
- 3dexample
- CORELIB_LP
- CORELIB_LP_LVT
- IOLIB_IL
- IOLIB_STRGD
- PadringLib
- US_8ths
- ahdlLib
- analogLib
- avTech
- basic
- cdsDefTechLib
- charteredFermiLibrary
- chrt013lp
- chrt013rf
- functional
- rfExamples
- rfLib

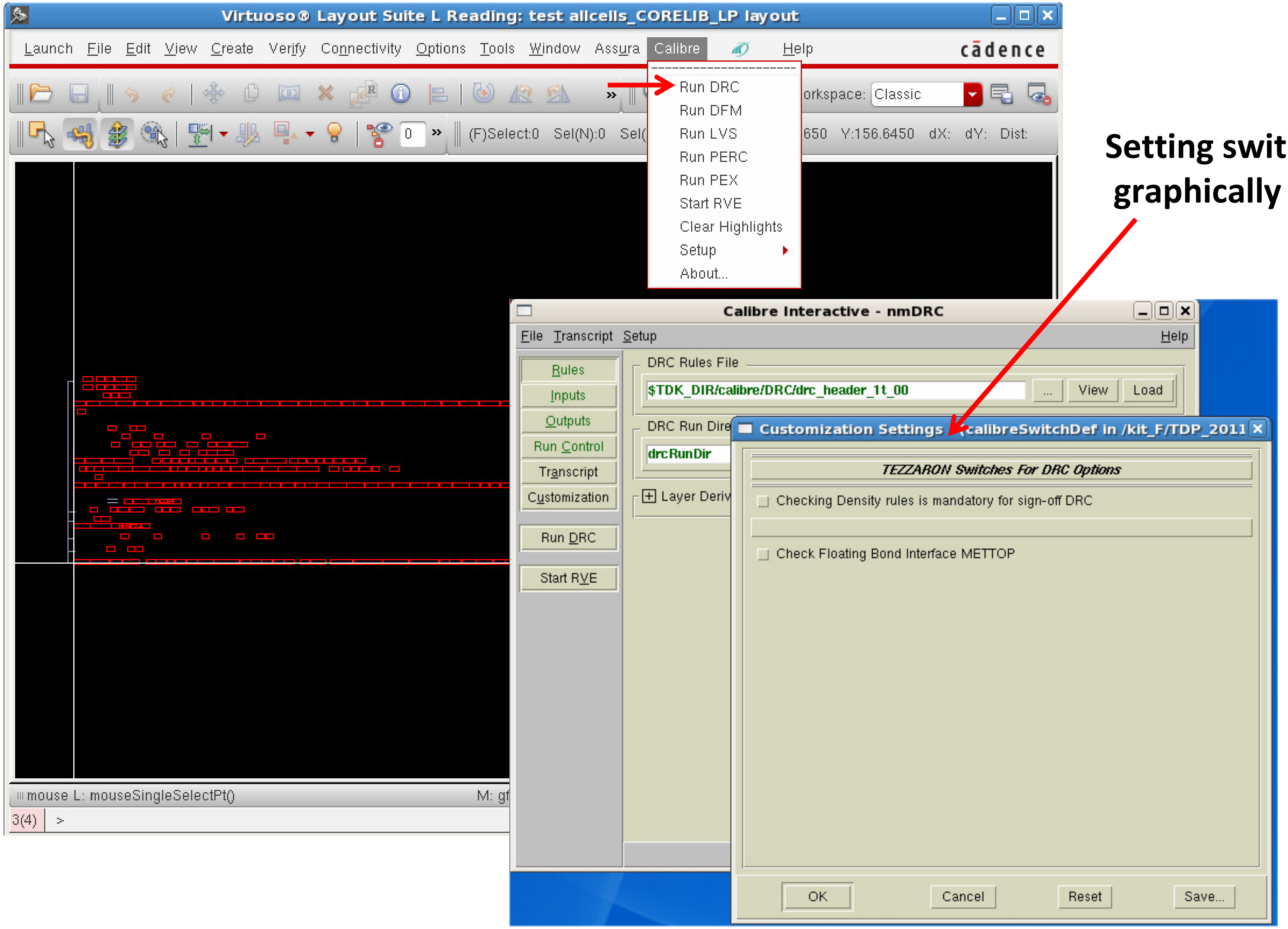
Category: AND

- Everything
- Uncategorized
- ADDERS
- AND
- AOI
- BOOTHENCODER
- BUFFERS
- CLOCK
- DELAYS
- FILLERS
- FLIPFLOPS
- INVERTERS
- LATCH
- LEAFCELLS
- MUX
- NAND
- NOR
- OAI
- OR
- OTHERS
- REGISTER
- SCANCELLS
- TRISTATE
- XNOR
- XOR

Cell

- AND2X1
- AND2X2
- AND2X4
- AND2X6
- AND2X8
- AND2XL
- AND3X1
- AND3X2
- AND3X4
- AND3X6
- AND3X8
- AND3XL
- AND4X1
- AND4X2
- AND4X4
- AND4X6
- AND4X8
- AND4XL

Virtuoso / Calibre DRC Interactive Menu



DRC Rules File: $TDK_DIR/calibre/DRC/drc_header_1t_00

DRC Run Directory: drcRunDir

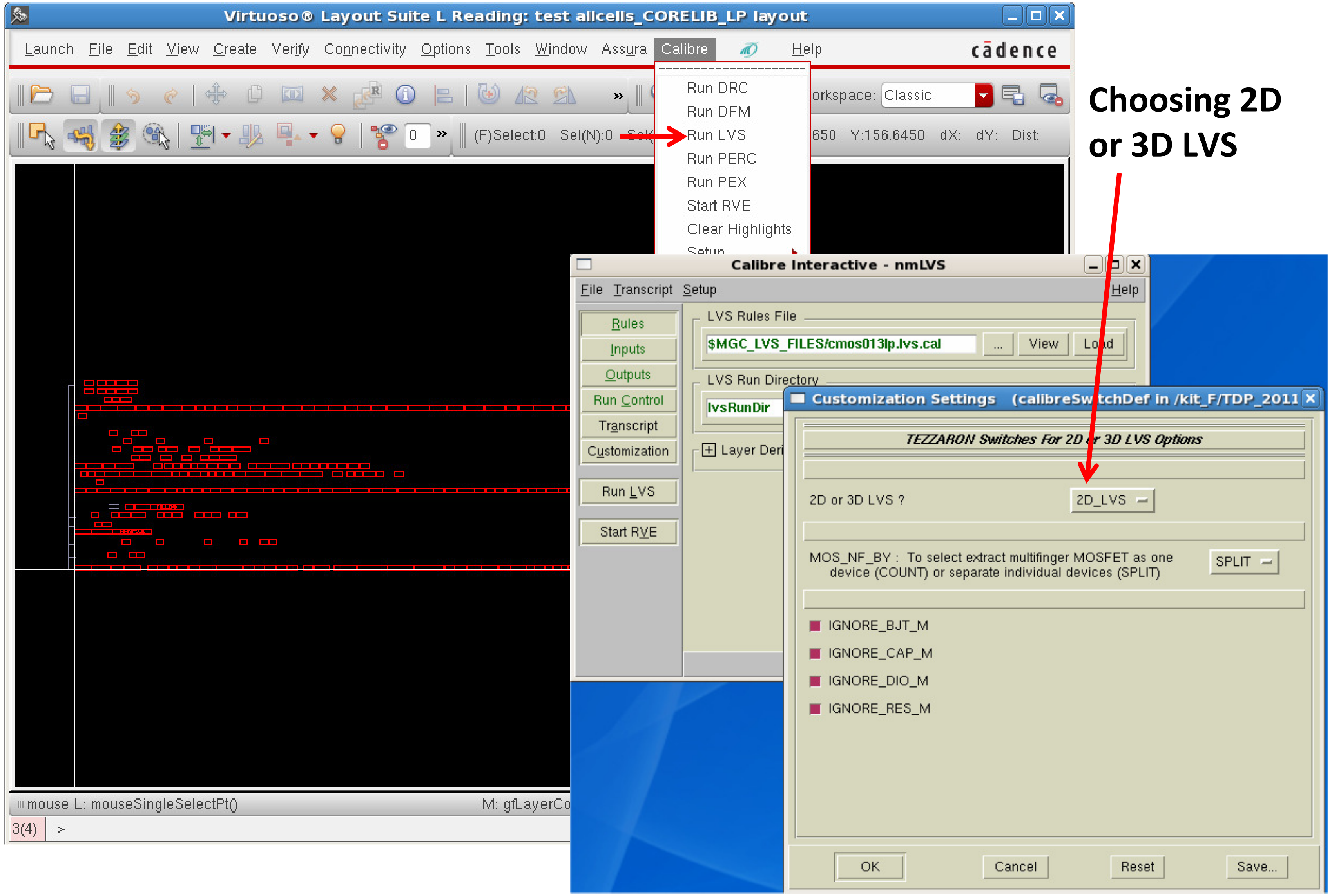
TEZZARON Switches For DRC Options

☐ Checking Density rules is mandatory for sign-off DRC

☐ Check Floating Bond Interface METTOP

Setting switches graphically

Virtuoso / Calibre LVS Interactive Menu



LVS Rules File: $MGC_LVS_FILES/cmos013lp.lvs.cal

LVS Run Directory: lvsRunDir

2D or 3D LVS ? 2D_LVS

MOS_NF_BY : To select extract multifinger MOSFET as one device (COUNT) or separate individual devices (SPLIT) SPLIT

- ■ IGNORE_BJT_M
- ■ IGNORE_CAP_M
- ■ IGNORE_DIO_M
- ■ IGNORE_RES_M

Choosing 2D or 3D LVS

New features in release 2011q2v3

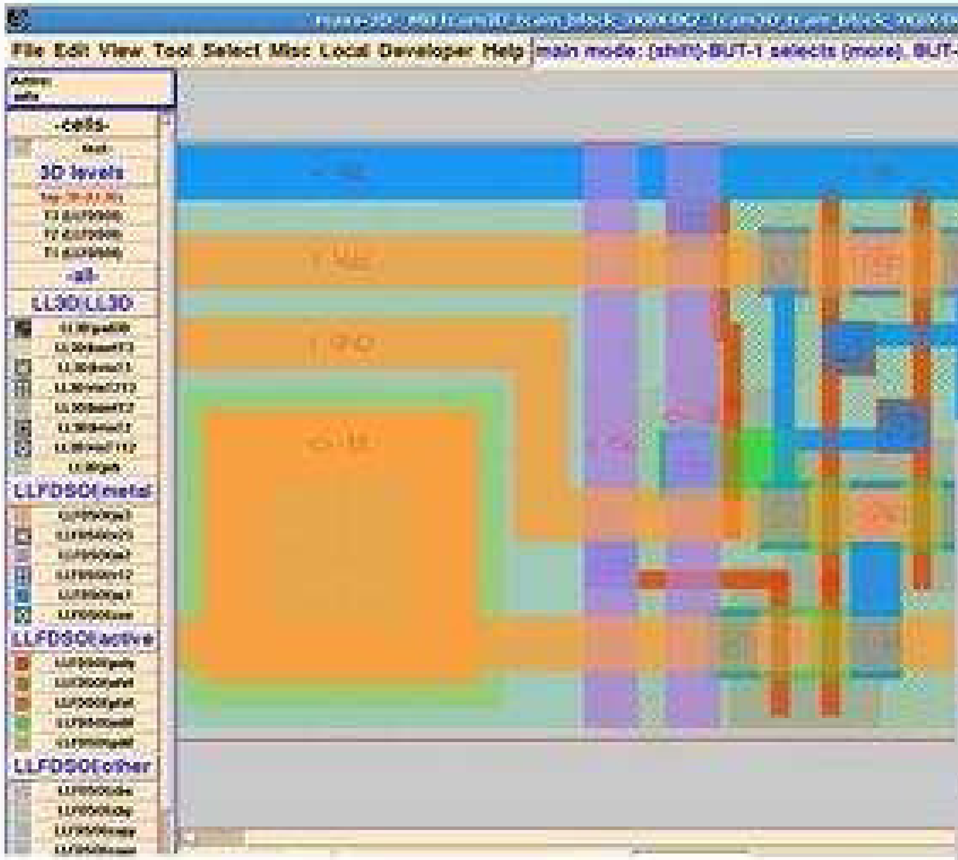
- 3D-LVS fully functional both for the CDB and OA.
- Graphical interface for the NCSU's preprocessor utility for merging 2 tiers GDSII.
- Corrected LEF file for the M6 / two thick metal option.
- Assura 2D LVS is functional.
- Walk-Through Encounter tutorial with both DBI and TSV scripting for automatic P&R.
- Master file browsing the documentation.

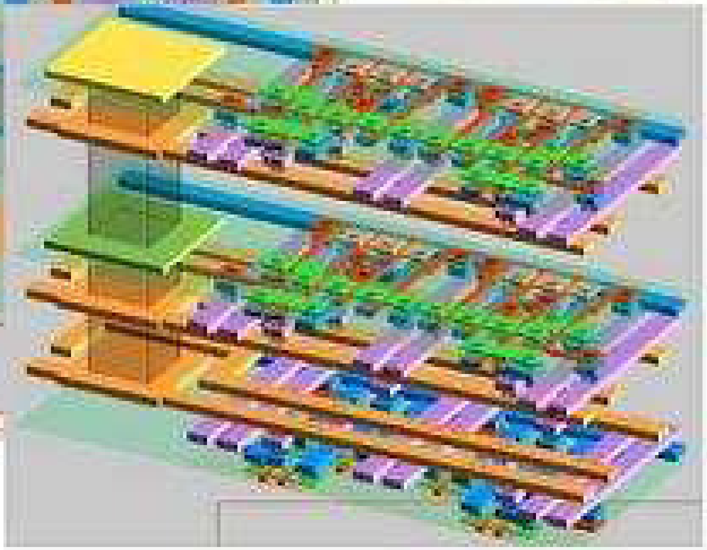
- 3 package options :
  - ✓ Complete design-platform TDP = (TDK + libraries + compilers)
  - ✓ TDK only
  - ✓ TDK + libraries with reduced layout views
    (memory blocks generated on request with reduced layout views)

True 3D Mask Layout Editor

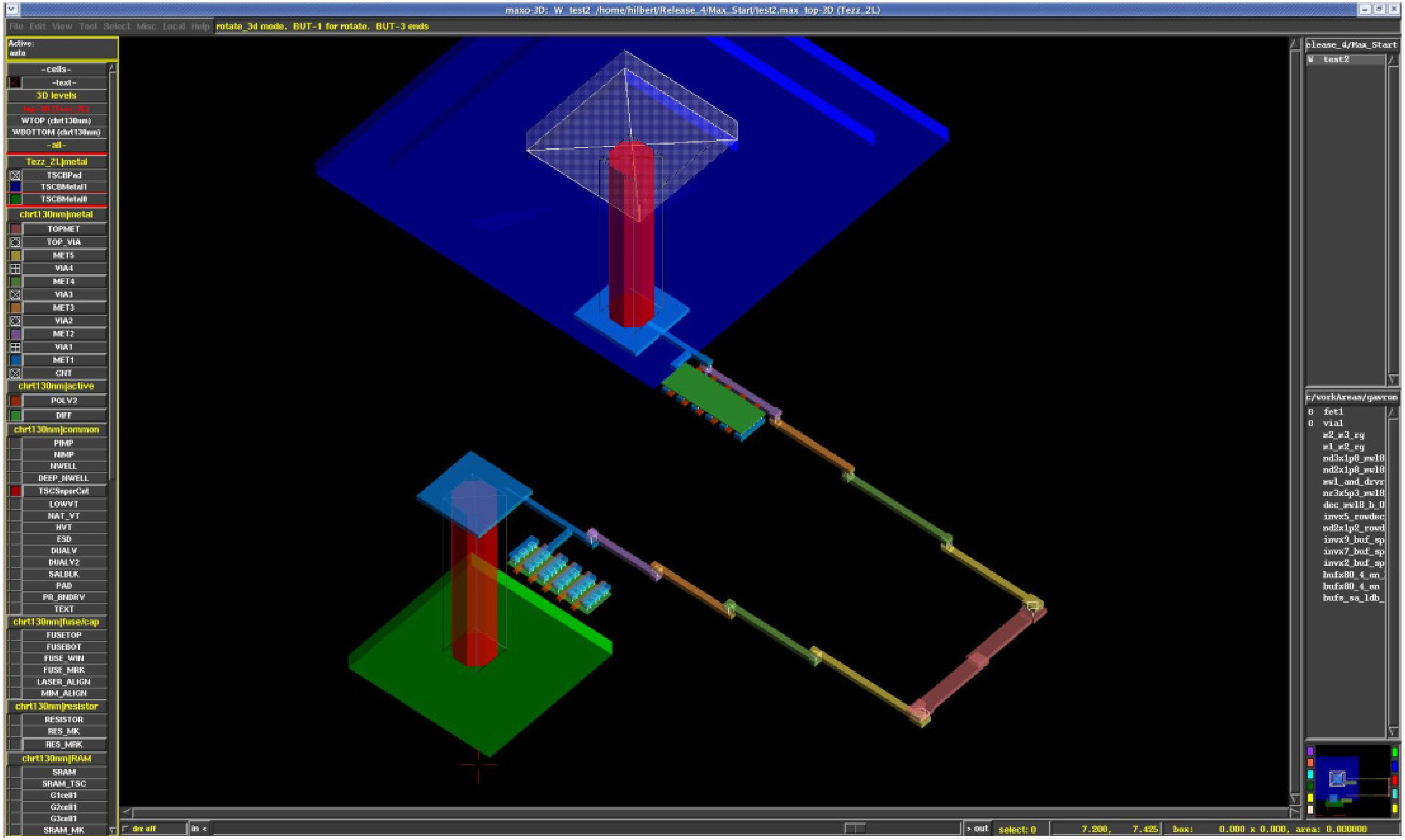
Technology Files fully supported by Tezzaron

MicroMagic MAX-3D





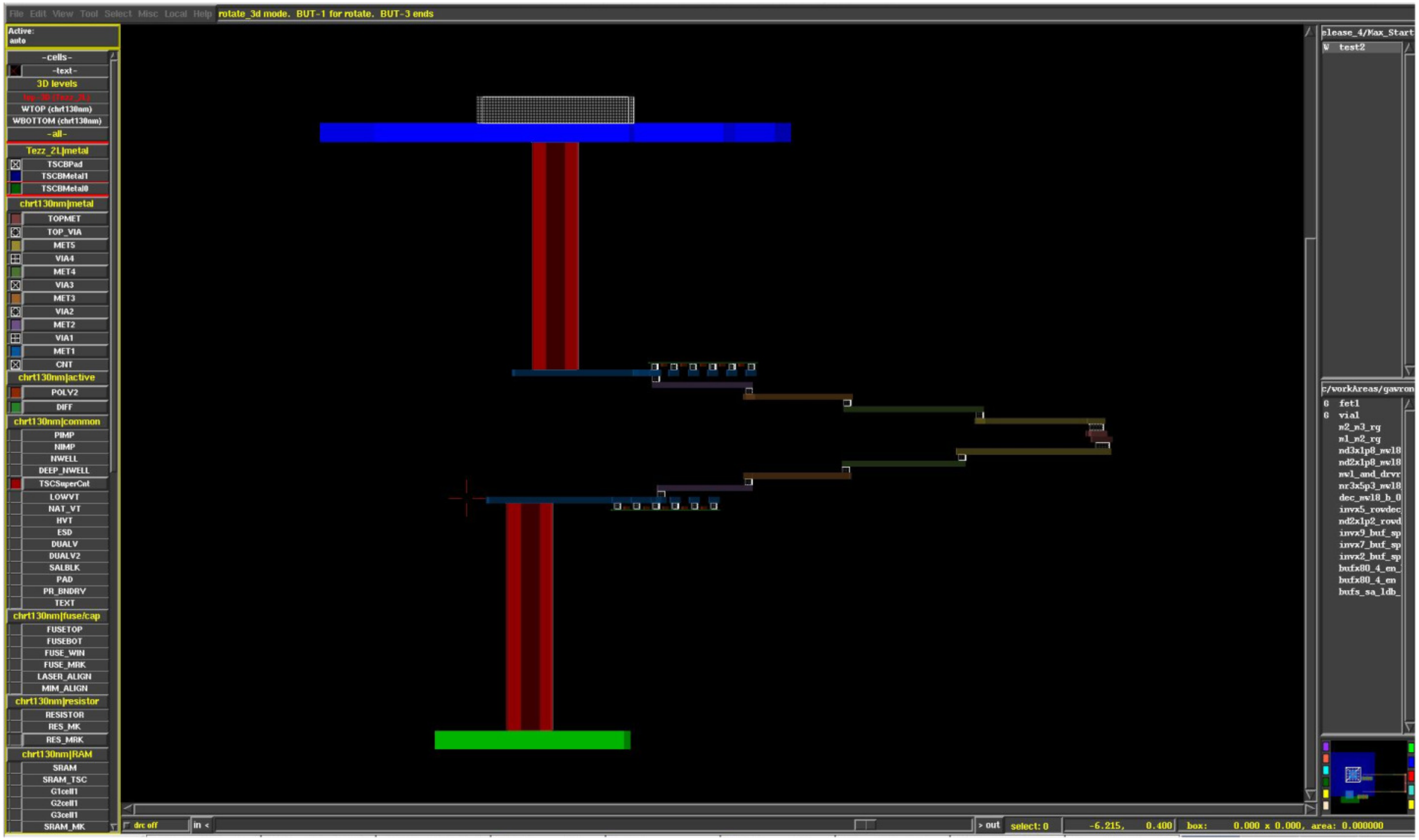
MicroMagic 3D viewer


maxo-3D: W test2 /home/hilbert/Release_4/Max_Start/test2.max top-3D (Tezz_2L)

rotate_3d mode. BUT-1 for rotate. BUT-3 ends

select: 0 7.200, 7.425 box: 0.000 x 0.000, area: 0.000000

MicroMagic 3D crossection


rotate_3d mode. BUT-1 for rotate. BUT-3 ends

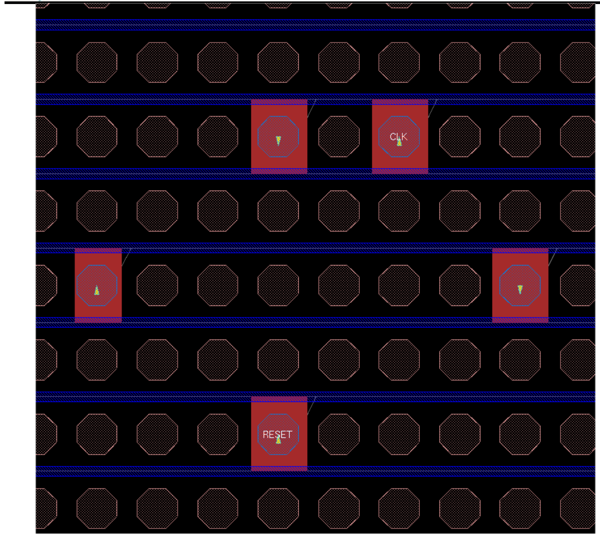
Active:
auto

select: 0   -6.215,   0.400   box: 0.000 x 0.000, area: 0.000000

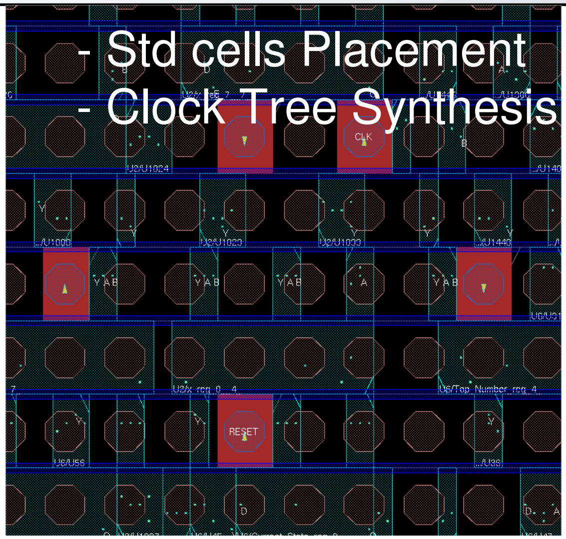
3D-IC Automatic P&R using DBI and TSV

System Level Partitioning	Design exploration at system level
3D Floor-Planning DBI, TSV, IO placement	Design exploration at the physical level DBI, TSV, and IO placement & optimization
Automatic Place & Route	Cells and blocks place & route can be done tier by tier
Extraction, Timing Analysis	To be done for each tier, then combined for back-annotation to the 3D top level system
Physical verification 3D DRC, 3D LVS	Similar to the full-custom design flow
Dummies Filling	
Final 3D DRC	

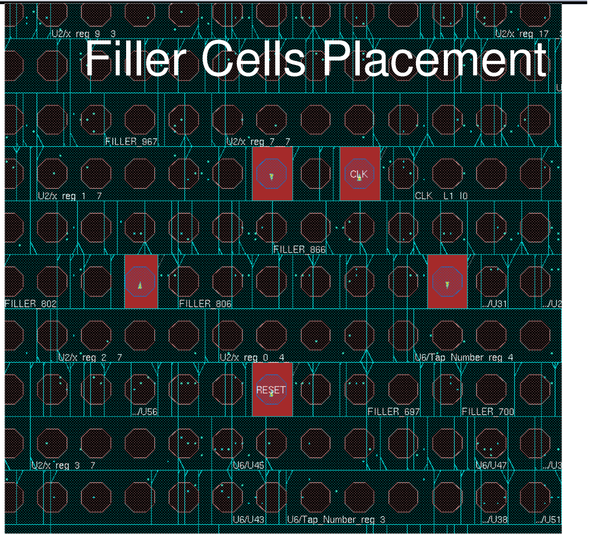
Automatic P & R Design Flow (From Floor-Plan to Routed Design)



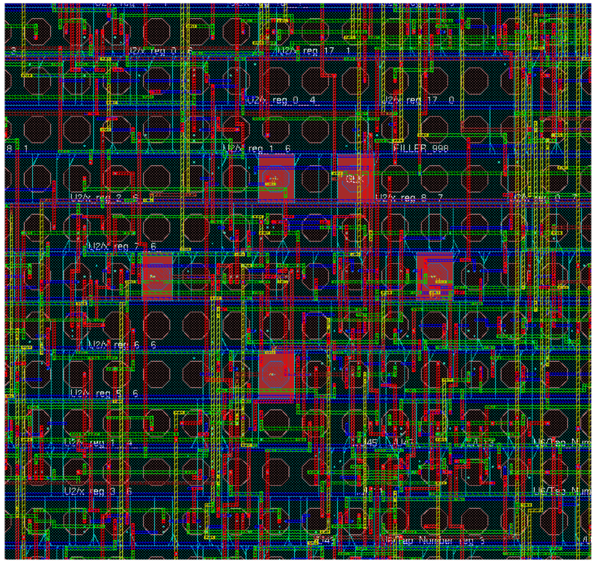
- DBIs Placement
- TSVs Placement
- Obstructions on TSVs



- Std cells Placement
- Clock Tree Synthesis



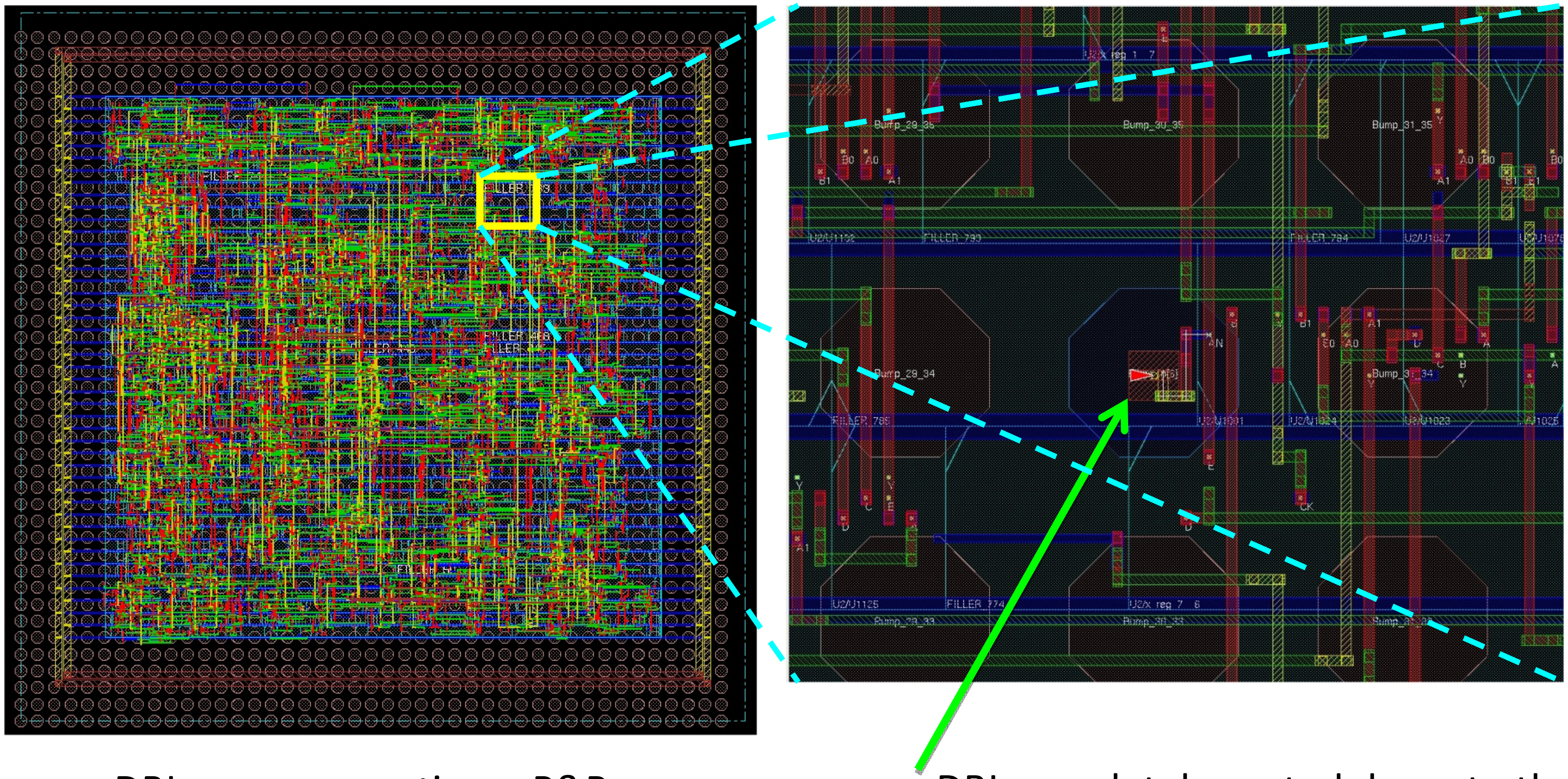
Filler Cells Placement



- Clock routing
- Final routing

Automatic P&R with Direct Bond Interface

- Encounter natively refuses to make the routing for pins on DBIs.
- Custom scripts solved the problem. It's a workaround.
- The resulting layout is compliant to the Tezzaron DRC, LVS etc …



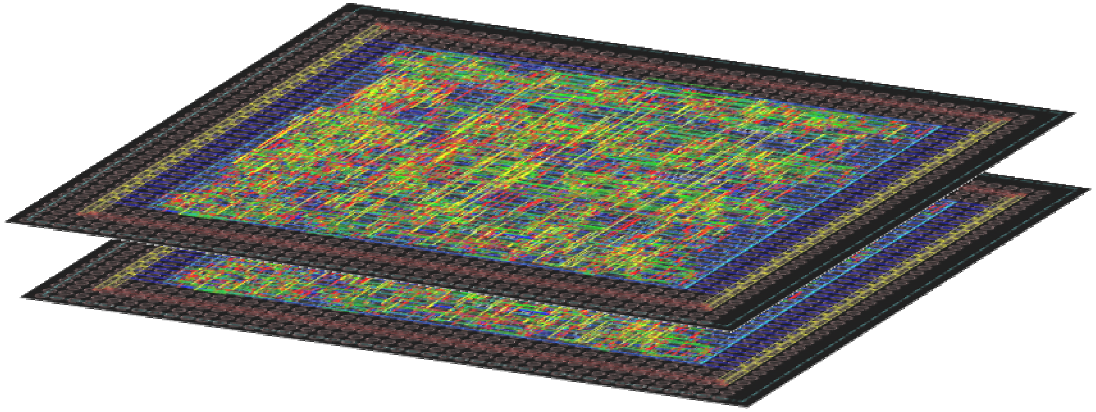
DBI array generation + P&R

DBI completely routed down to the lower metal layers

Automatic P&R with Direct Bond Interface

Saving the floor plan for the bottom tier, and apply it for top tier so the automatic Place & Route run the placement and routing taking into account the DBI locations.

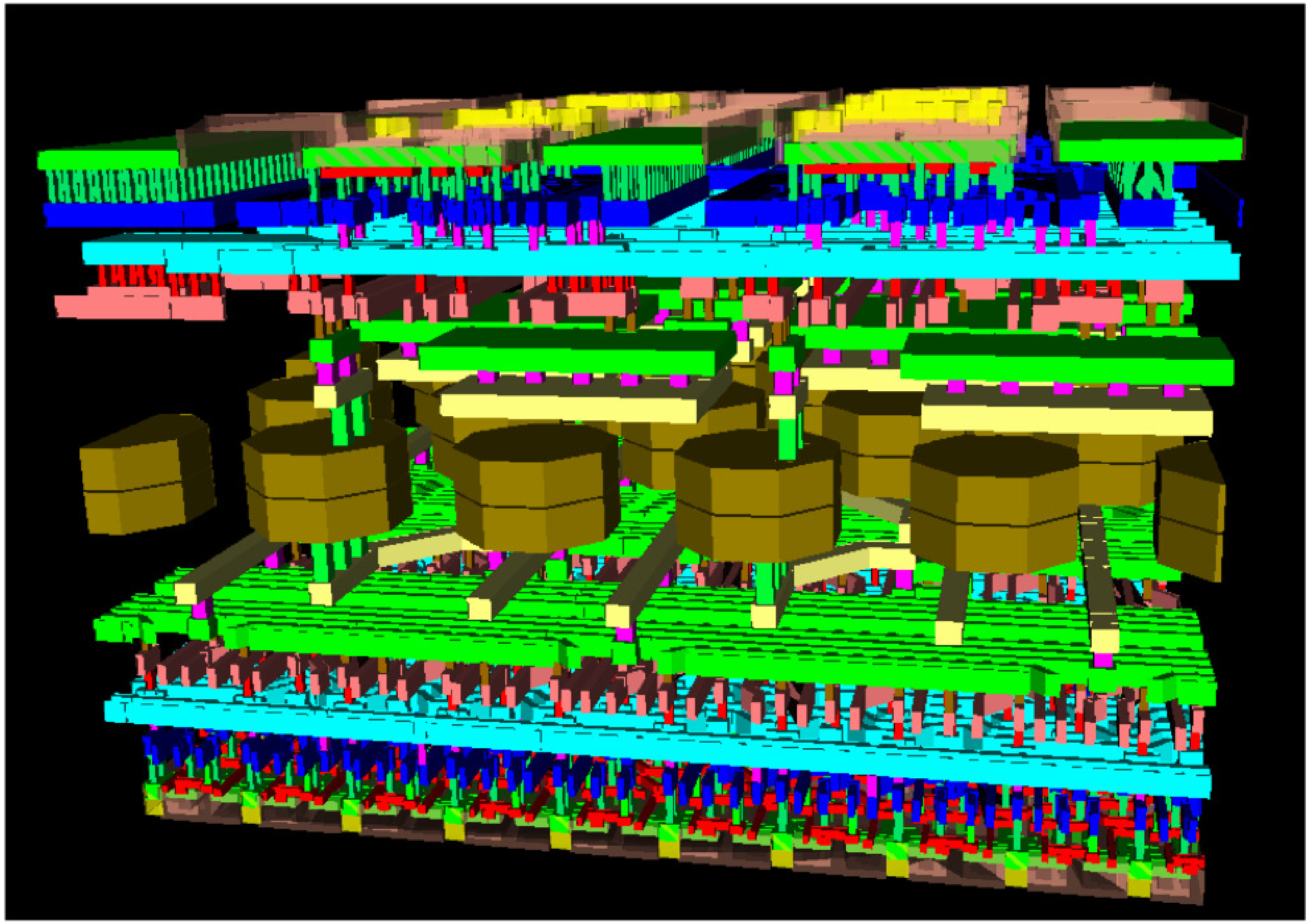
The place & route for both tiers is optimal for timing, buffer sizing and power performance.



Resulting in a "correct by construction" design.

3D viewer for 3D-IC design

- Graphically Interfaced into Virtuoso.
- Works for both CDB and OA.
- Use a free and open-source VRML viewer.



MPW run in 2011

- First MPW run Tezzaron 3D-IC 130nm. October 2011.

Institution	Town	Country	Area
DEUTSCHES ELEKTRONEN-SYNCHROTRON (DESY)	HAMBURG	GERMANY	19.7 mm^2
LAL / IN2P3 / CNRS	ORSAY	FRANCE	25 mm^2
ISEA	Toulouse	FRANCE	6.25 mm^2

Conclusion

- ☐ A very collaborative work has been achieved and still ongoing between the partening CMC, CMP, MOSIS, FermiLab, Tezzaron, HEP Labs, NCSU.

- ☐ Design Platform **2011q2v3** in use since June 2011.