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Memory leads the way to better computing

H.-S. Philip Wong and Sayeef Salahuddin

New non-volatile memory devices store information using different physical mechanisms from those employed in today's memories and could achieve substantial improvements in computing performance and energy efficiency.

Current memory devices store information in the charge state of a capacitor; the presence or absence of charges represents logic 1's or 0's. Several technologies are emerging to build memory devices in which other mechanisms are used for information storage. They may allow the monolithic integration of memories and computation units in three-dimensional chips for future computing systems[1]. Among those promising candidates are spin-transfer-torque magnetic random access memory (STT-MRAM) devices, which store information in the magnetization of a nanoscale magnet. Other candidates that are approaching commercialization include phase change memory (PCM), metal oxide resistive random access memory (RRAM) and conductive bridge random access memory (CBRAM).

Today's computing systems use a hierarchy of volatile and non-volatile data storage devices to achieve an optimal trade-off between cost and performance[2]. The portion of the memory that is the closest to the processor core is accessed frequently, and therefore it requires the fastest operation speed possible; it is also the most expensive memory because of the large chip area required. Other levels in the memory hierarchy are optimized for storage capacity and speed (Fig. 1). The main memory is often located in a separate chip because it is fabricated with a different technology from that of the microprocessor.

For over 30 years, static random access memory (SRAM)[3] and dynamic random access memory (DRAM)[3] have been the workhorses of this memory hierarchy[4]. Both SRAM and DRAM are volatile memories — that is, they lose the stored information once the power is cut off. For non-volatile data storage, magnetic hard disk drives (HDDs) have been in use for over five decades[5–7]. Since the advent of portable electronic devices such as music players and mobile phones, however, solid-state non-volatile memory known as Flash memory[8] has been introduced into the information storage hierarchy between the DRAM and the HDD. Flash has become the dominant data storage device for mobile electronics; increasingly, even enterprise-scale computing systems and cloud data storage systems are using Flash to complement the storage capabilities of HDD.

Resistive switching memory technologies

The design specifications for memory (volatile data storage, fast, expensive) and for storage (non-volatile data storage, slow, inexpensive) are different, and they often have different data access standards and protocols. Around 15 years ago, researchers started exploring the possibility of blurring the design boundary between memory and storage[9,10], and coming up with new data access modes and protocols that are neither 'memory' nor 'storage'. Indeed, the adoption of Flash in the memory hierarchy (albeit on a separate chip from the processor) inspired the exploration of computing architectures that capitalize on the salient features of Flash: non-volatility and high density[11]. At the same time, new types of non-volatile memory have emerged that can easily be integrated on-chip with the microprocessor cores because they use a different set of materials and require different device fabrication technologies from Flash[12]. Some of them can be programmed and read quickly; others can have very high data storage density. Importantly, all of these memories are free from the limitations of Flash — that is, low endurance, need for high voltage supply, slow write speed

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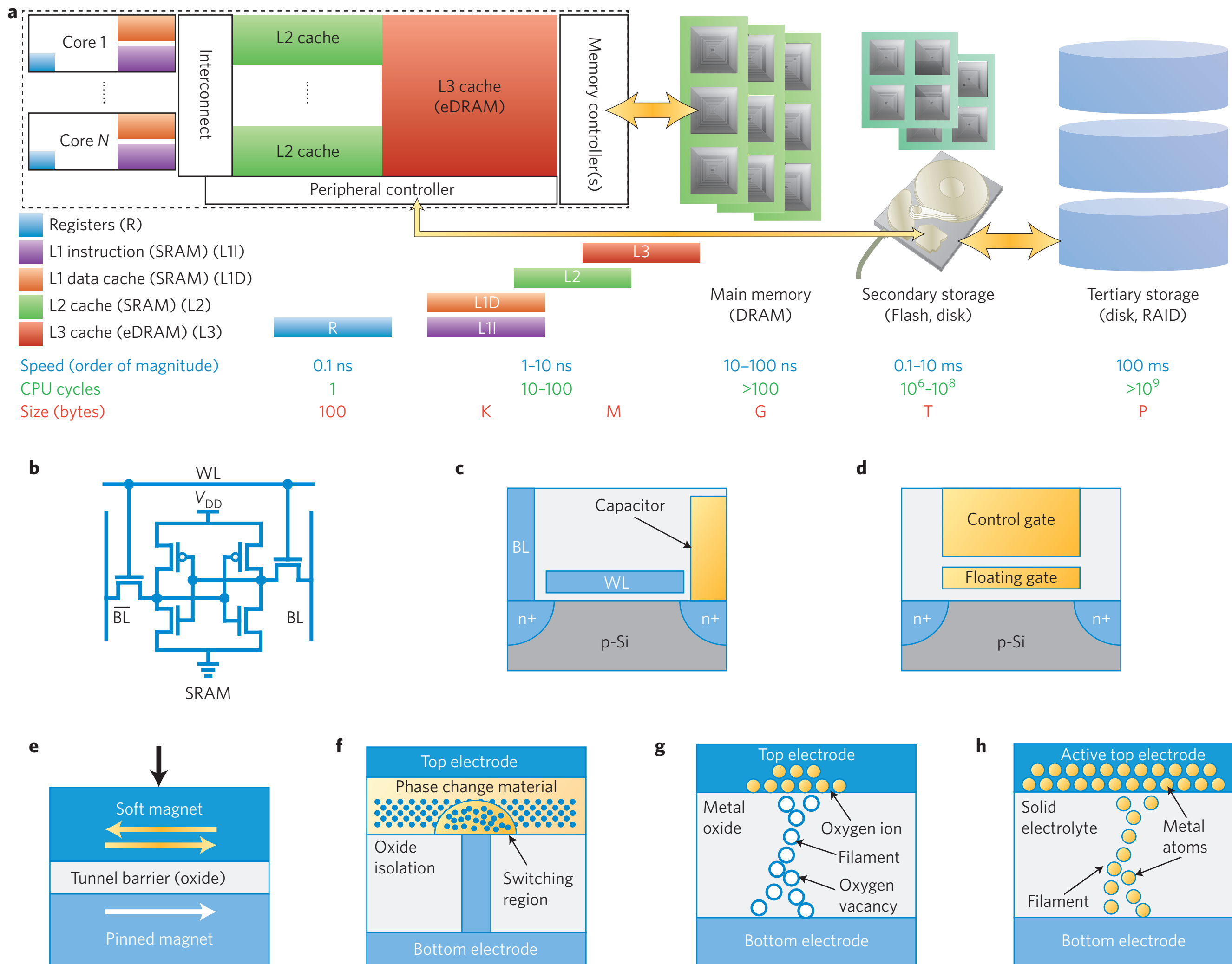

Figure 1 | Memory hierarchy and various memory types. **a**, Physical distribution and hierarchy of memory in a computer. The lower panel shows speed (as order of magnitude), number of processor (CPU) cycles needed to access the memory, and size of the different memories. RAID, redundant array of independent disks. **b**, Schematic of a circuit of a SRAM cell consisting of six transistors. BL, bit line; $\overline{BL}$, logic complement of BL; WL, word line; V_{DD}, supply voltage. **c–h**, Schematics of DRAM (**c**), Flash (**d**), STT-MRAM (**e**), PCM (**f**), RRAM (**g**) and CBRAM (**h**). The black downward arrow in **e** indicates the direction of current flow.

and cumbersome erase procedure. Coincidentally, these new memories store information using new types of physics that do not rely on storing charge on a capacitor as is the case for SRAM, DRAM and Flash.

Spin-transfer-torque magnetic random access memory. The basic physics of operation of STT-MRAMs is discussed by Kent and Worledge[13]. Here, we focus on the aspect of scaling and its relation to the data retention time of this technology. In a ferromagnet, spin up and spin down states are separated by a well-defined energy barrier (E_B). A loss of memory happens when a state spontaneously flips to the other by overcoming E_B, for example by absorbing energy from the thermal bath. A performance metric for STT-MRAM is therefore $\Delta = E_B/k_BT$ (k_B, Boltzmann constant; T, temperature) such that the memory retention time is given by $\tau = \tau_0 \exp(\Delta)$. The retention time τ_0 is typically of the order of 1 ns. E_B depends on the energy stored in the magnet. To switch a ferromagnet, one needs to supply it with an amount of energy that is at least equal to E_B; thus, within this simple scenario, the switching current — and therefore the write energy — is proportional to E_B and varies in a logarithmic fashion with the required retention time. For a memory array, statistical considerations lead to an increase in the required value of Δ (ref. 14), but the simple relation shown above provides a reasonable insight.

It is noteworthy that such a one-to-one relation between write current and retention time is not common to the other emerging technologies and provides an important design tool for STT-MRAMs. Although the traditional industry standard is a retention time τ of around 10 years, for most modern-day RAM applications this standard is simply irrelevant. In particular, for embedded memory applications, a much smaller τ (even in the range of seconds, depending on application) could be sufficient, allowing significant reduction in the energy needed for the write operation by trading-off in reduced retention times. In embedded applications where the computing system is normally in the off state and requirements on speed are relaxed, such design optimizations — combined with an appropriate architecture that exploits the non-volatility — could lead to significant performance improvements. In addition, emerging all-spin schemes[15–17] that combine logic and memory devices in the same structure could lead to significant energy savings and increase in data storage density.

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Phase change memory. In PCM, two electrodes sandwich a chalcogenide glass that can change between the crystalline and amorphous phase on heating and cooling. Such phase changes are induced by passing a current through the material to heat it up. Information is stored in the phase of the active material; crystalline or amorphous phases have a different resistance *R* and correspond to the two logic states. One of the advantages of PCM[18] is that materials that have been extensively studied[19] and that can be mass produced can be used, for example in DVDs. The resistance ratio between the amorphous phase and the polycrystalline phase is over 100 times larger than in STT-MRAM devices. Thus, multi-bit storage might seem achievable; however, in phase change materials the amorphous intermediate resistance states drift with time, *t*, towards higher resistance, following a $R(t) = R_0(t/t_0)^\nu$ power-law relationship (R_0 is the resistance at t_0; ν is material- and device-dependent), thus making it difficult to distinguish the programmed states over time. Because PCM is programmed by Joule heating, the programming current scales down with device area. Programming current of the order of microamps is shown to be possible when the device area is scaled to sizes smaller than 10 nm (ref. 20). Advances in the development of materials that are based on superlattices, and switch phase without melting, promise to push the programming current even lower[21].

Metal oxide resistive random access memory. In devices of this type, a metal oxide is sandwiched between two metal electrodes. An applied electric field induces the creation and motion of oxygen vacancies, resulting in the formation of conductive filaments in the oxide. This changes the device resistance, which varies between high and low states. Industry has high hopes for RRAM[22–24] because it uses materials that are common in semiconductor manufacturing. Typical metal oxides include HfO_x, TaO_x, TiO_x and AlO_x, all of which can be deposited using atomic layer deposition. Although the device concept is simple, the physics is anything but. There are controversies surrounding the shape of the conductive filament and the role of the top and the bottom electrodes. The mobility, energy and stability of the oxygen vacancies remain topics of intense study[22]. As a result of these open issues, projection of device reliability becomes difficult. Furthermore, RRAMs have issues of reproducibility of their electrical characteristics; there are large resistance variations not just between devices, but also between cycles of programming of the same device. This problem has been holding RRAM back from commercialization despite its many attractive features. However, the ease with which RRAM can be built in three dimensions is yet another strong incentive to develop this technology further[25].

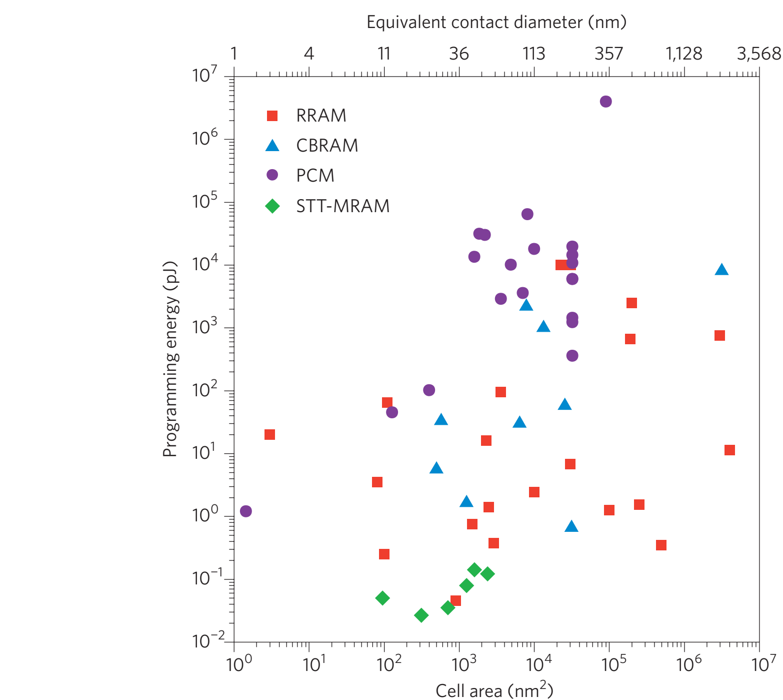

Figure 2 | A comparison of a key attribute (write energy versus device size) of emerging non-volatile memories. Data from ref. 35.

Conductive bridge random access memory. This type of memory[26] is a close cousin of RRAM, in which the metal oxide is replaced by a solid electrolyte and one of the electrodes is a metal that can easily oxidize into metal ions. On application of an electric field, mobile metal atoms from the top (active) electrode migrate into the solid electrolyte to form conductive filaments that bridge the bottom electrode. Because of the stochastic migration process, the configuration of the conductive filament changes every time it is re-formed and results in large resistance variations similar to those in RRAM. The switching voltages of early CBRAM were too low (<0.5 V) (ref. 22), which led to poor retention. A recent work[27] shows significant improvement in both the switching voltage and resistance variation.

Energy, performance, scalability

Phase change memory has much better endurance (~10^9 cycles) than Flash and can easily achieve multi-bit data storage. The writing speed of PCM in the tens of nanoseconds and its relatively large programming current at today's feature size of tens of nanometres make it less attractive than STT-MRAM, RRAM and CBRAM. STT-MRAM excels in endurance cycling and speed, but its low resistance ratio requires a memory cell architecture that limits its device density. RRAM and CBRAM have endurance on a par with or better than PCM, and higher speed (of the order of nanoseconds), but suffer from resistance variation far worse than that of PCM and STT-MRAM. All these memories promise to scale further than Flash and DRAM (Fig. 2).

When these emerging memories were initially proposed, there was hope that one of them would be able to serve the entire memory hierarchy, meeting the need for power, energy, retention, endurance and speed required at each level; it was also envisaged that these memories could achieve high device density at low cost and be scalable for many technology generations — essentially that they could become a 'universal memory'[28–30]. Now it is generally agreed that the vision of a 'universal memory' is not realistic. Application-driven design requires the optimization of performance at each level of the memory hierarchy, and this requires trade-offs in device characteristics that span many orders of magnitude; this is fundamentally hard to achieve by any individual device technology. For example, the need for low energy consumption during writing operations is

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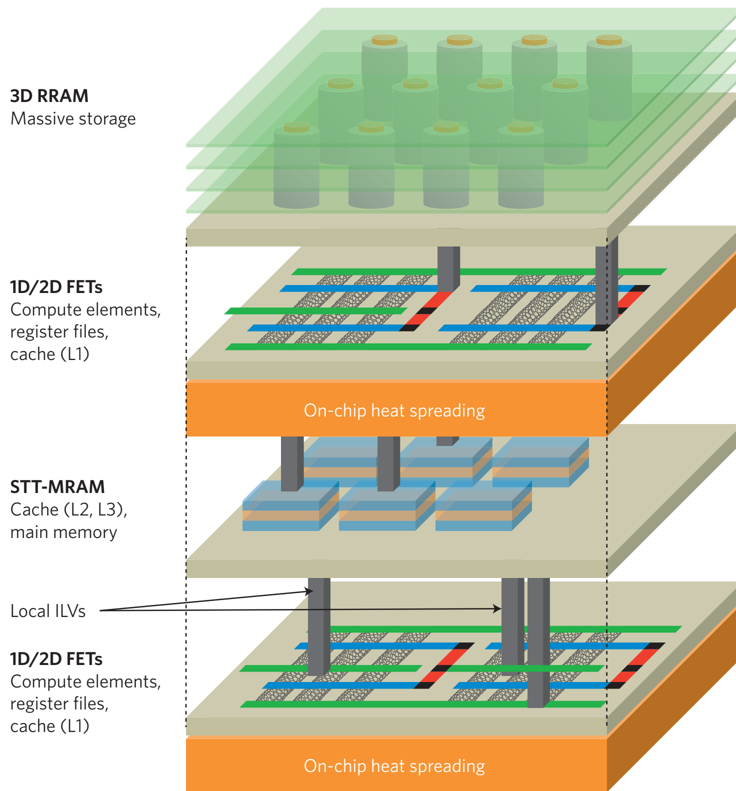

Figure 3 | Monolithic 3D integration of memory interleaved with logic computation layers. ILV, interlevel via; FET, field-effect transistor. Figure adapted with permission from ref. 36, IEEE.

accomplished by lowering the energy barrier to be overcome when erasing or writing data, which limits the non-volatile retention time of data.

Bring memory closer to computation

Shuttling data between the various levels of memory hierarchy incurs substantial latency and energy costs[4,31]. The effectiveness of the memory hierarchy depends on data locality — data in cache memories are accessed and reused frequently. For twenty-first century applications such as big-data analytics, processing of large graphs in real time and other emerging machine-learning tasks, the memory capacity required is enormous, and the memory locations are accessed in an unpredictable order. The processor often cannot find the data needed in cache memory. Because it takes many processor (central processing unit, CPU) cycles to fetch data from the main memory (Fig. 1), the CPU may stall through unavailability of data, resulting in loss of performance and power efficiency. The lack of data locality associated with important applications as mentioned above demands a different approach from the conventional one.

New memory technologies offer a unique opportunity to bring large amounts of memory closer to the computing elements, resulting in high-bandwidth, low-latency access. This is because all the emerging memory technologies described above can be fabricated at low temperatures and integrated monolithically in a three-dimensional (3D) chip; the relatively small thickness of these devices means that very short, high-density interlevel vias can be used to connect the memory with the computing units and the memory controller circuits (Fig. 3). Memory can also be woven into logic layers in a fine-grain fashion[32]. Significant improvements in energy-delay product (a measure of energy efficiency) can be achieved using this approach[1]. When memory layers are interleaved and woven with the logic computation layers, long-distance data movement is eliminated. Logic layers that support this monolithic 3D vision are beginning to emerge, as 1D carbon nanotube transistors[33] and 2D layered transition metal dichalcogenide transistors[34] advance from prototype devices to circuit and system demonstrations.

With the ability to tightly integrate massive amounts of memory with logic, it is conceivable that future computing chips may be much more compact and energy efficient than they are today. ❐

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