Cooling Three-Dimensional Integrated Circuits using Power Delivery Networks (PDNs)

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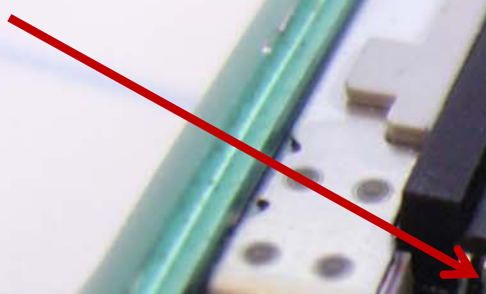
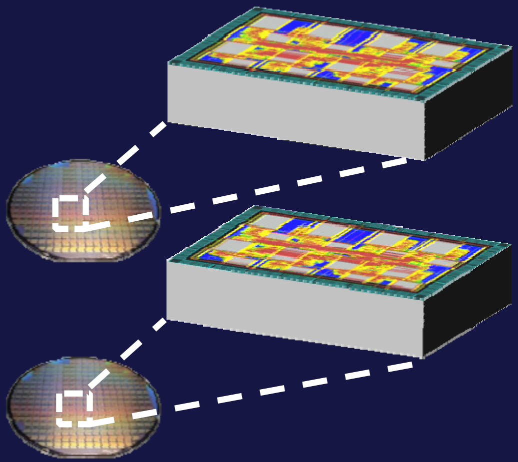
Stanford University, Rambus+, MonolithIC 3D Inc.*

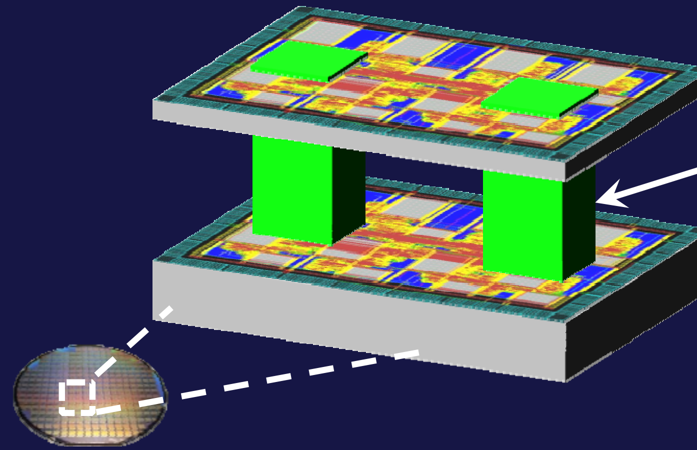
Acknowledgement: FCRP C2S2, NSF


3D IC

3D Integration

Parallel 3D

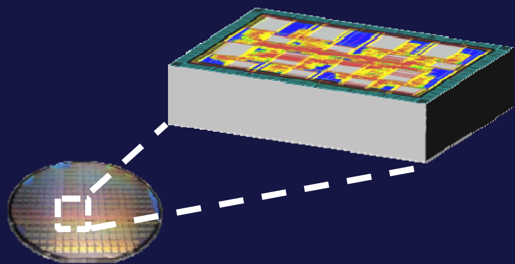


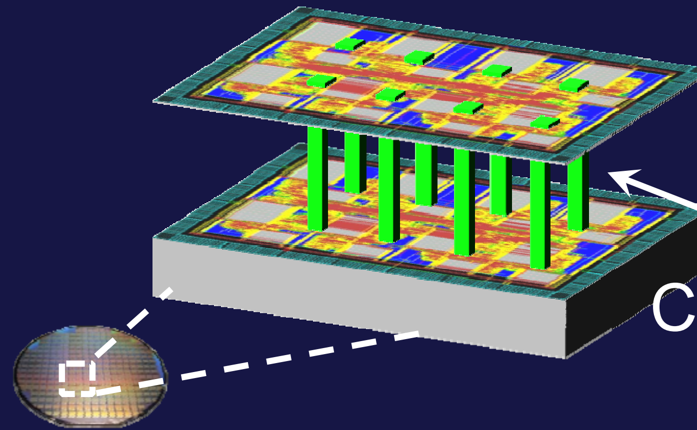


TSVs

Integration

Sequential (Monolithic) 3D

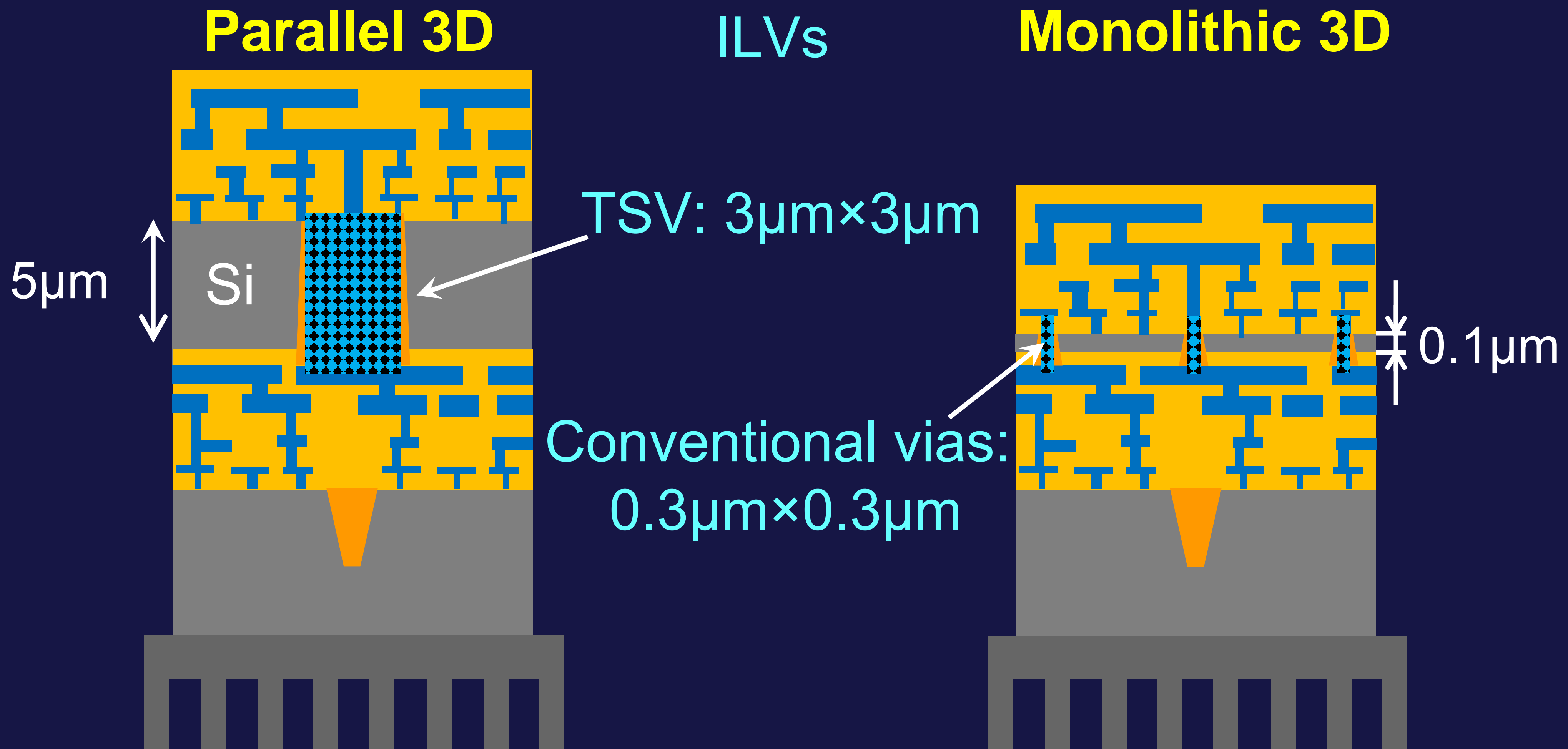




Conventional vias

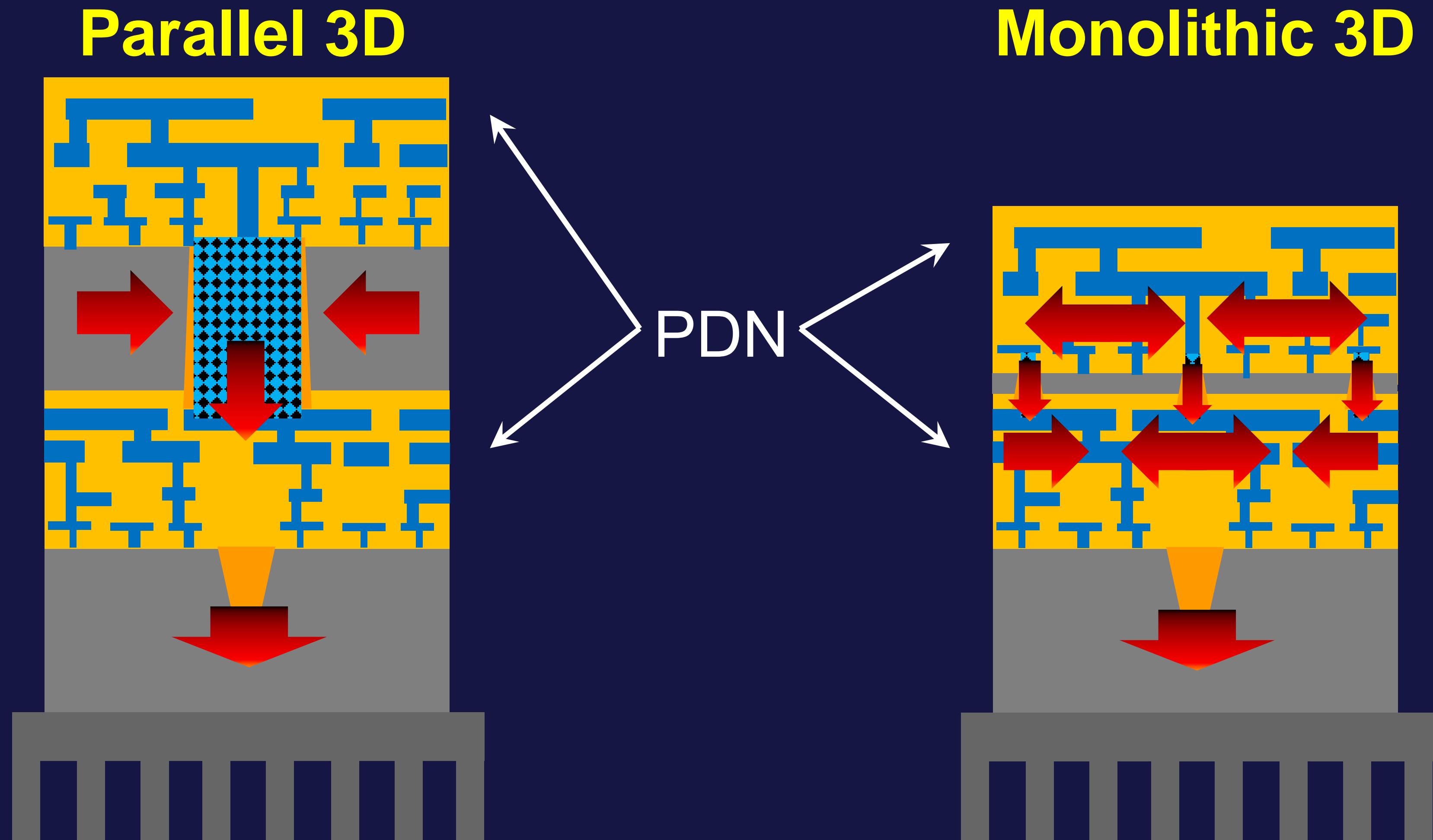
Geometries

- ILV: Inter-Layer Via

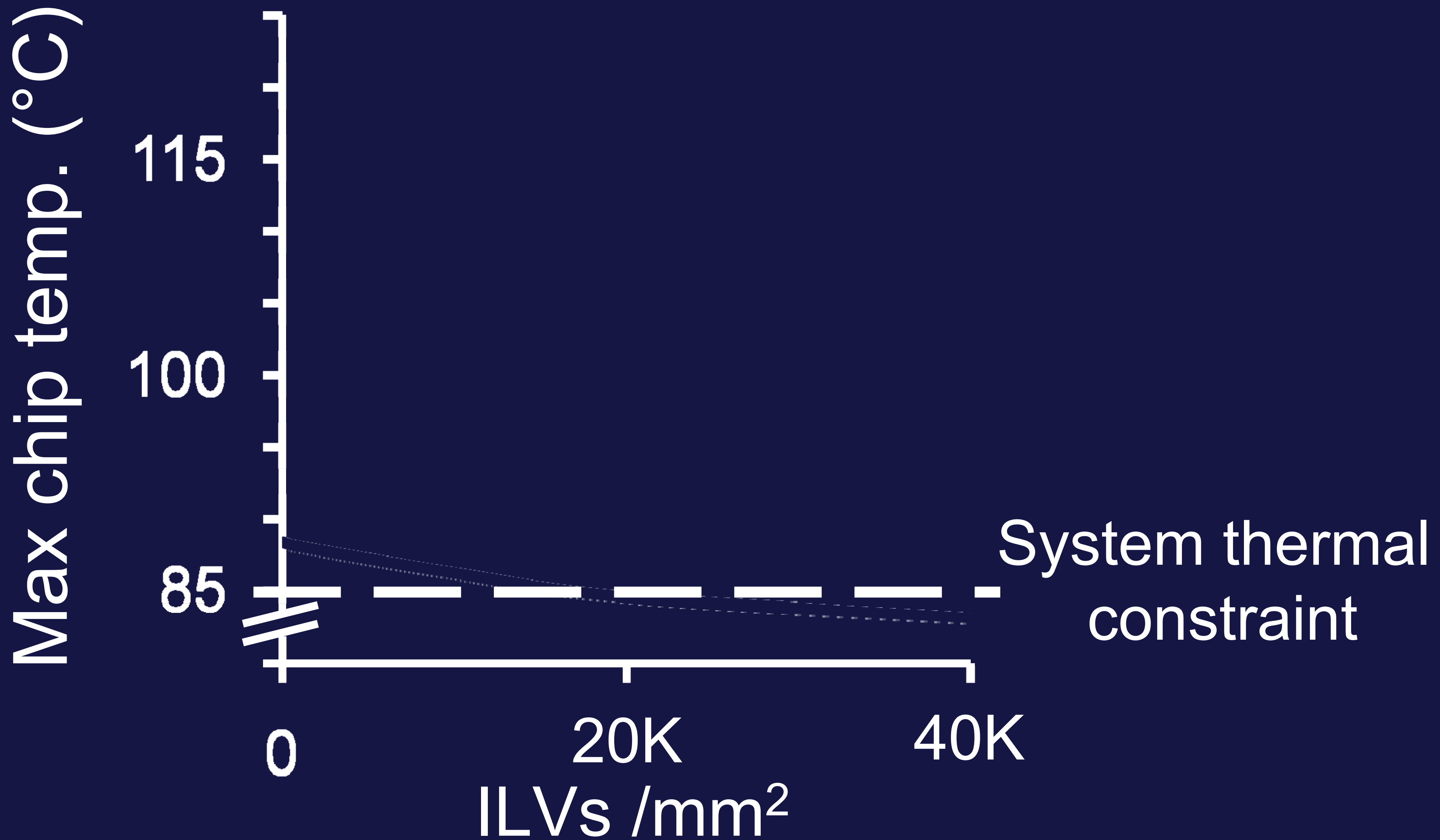


Geometries

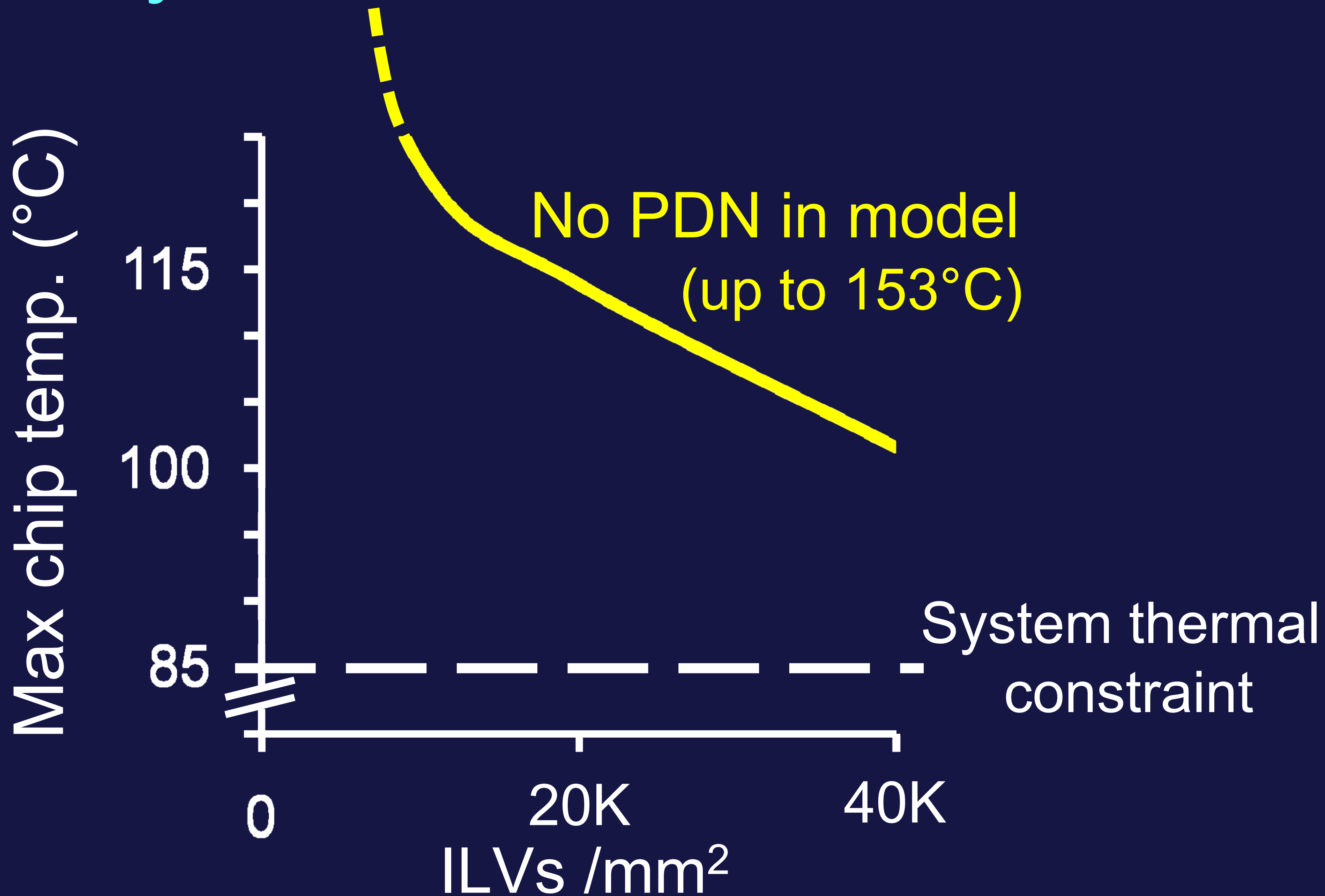
- PDN: Power Delivery Network



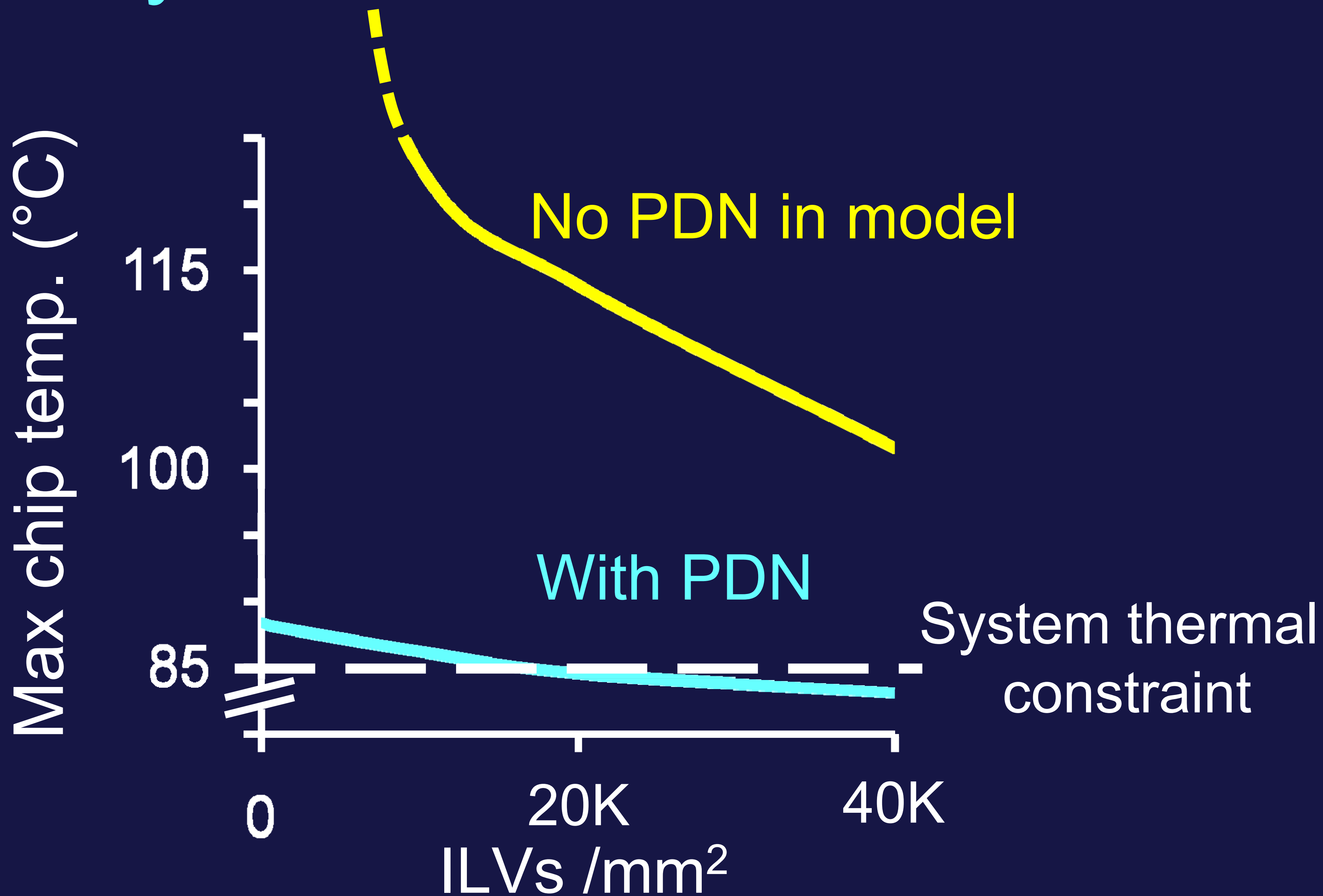
Key Result for Monolithic 3D



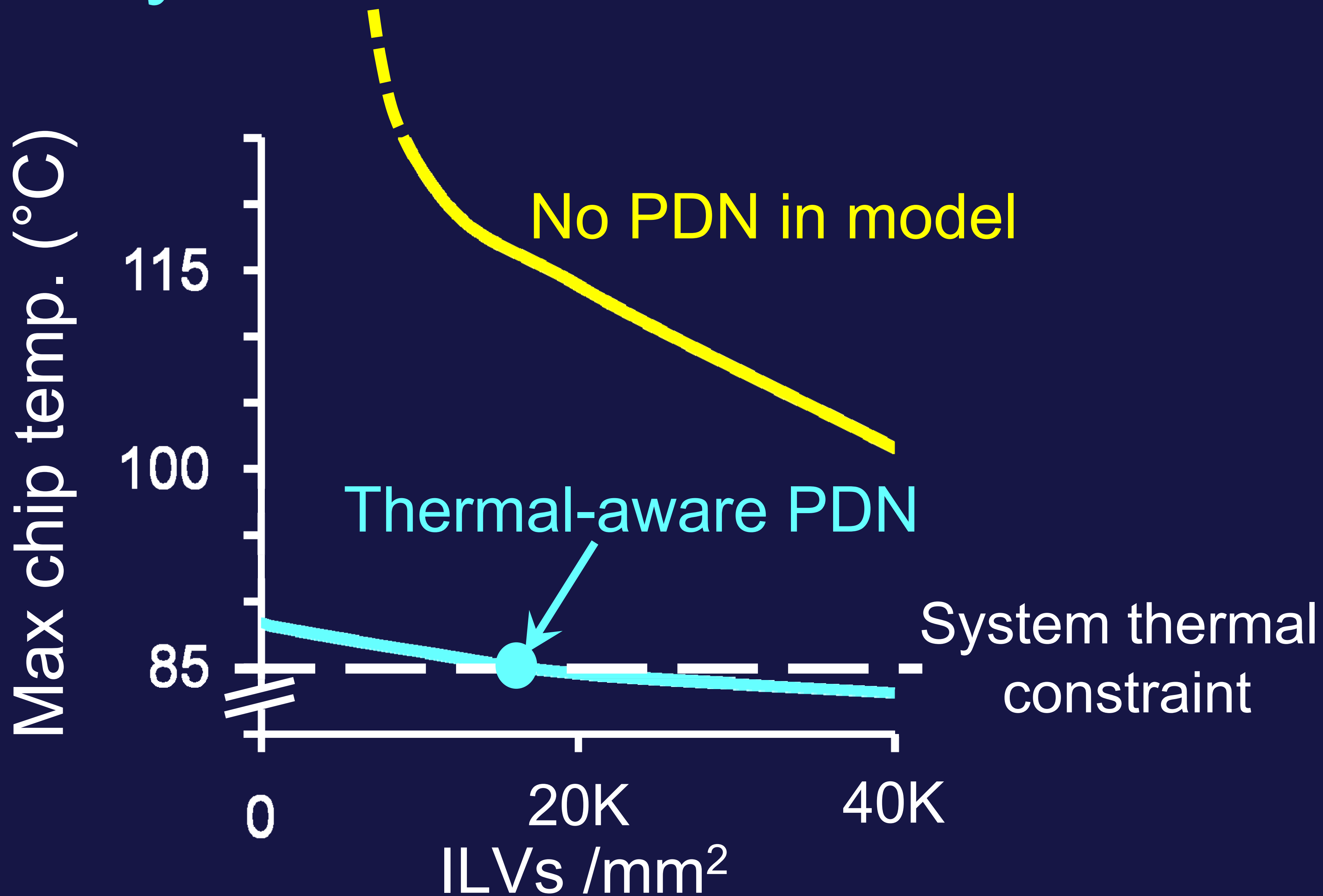
Key Result for Monolithic 3D



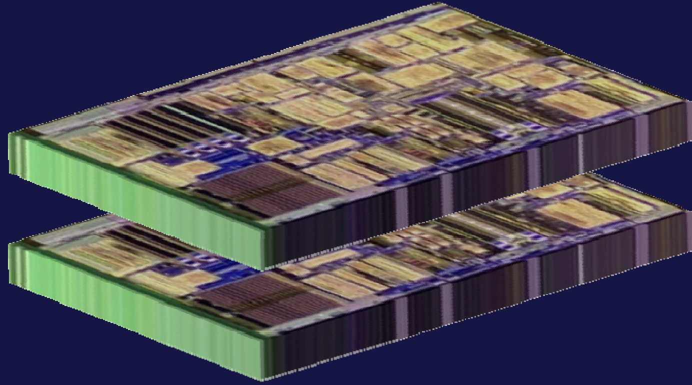
Key Result for Monolithic 3D



Key Result for Monolithic 3D



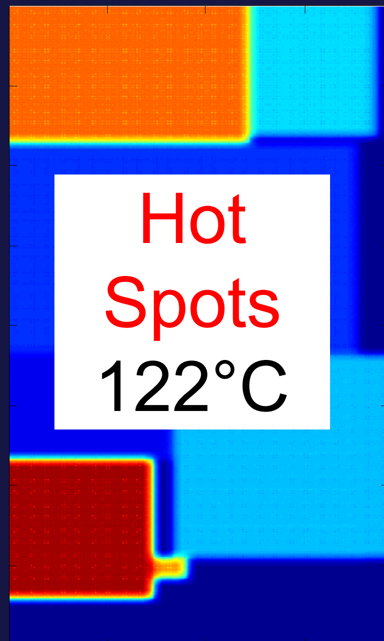
Key Result for Monolithic 3D

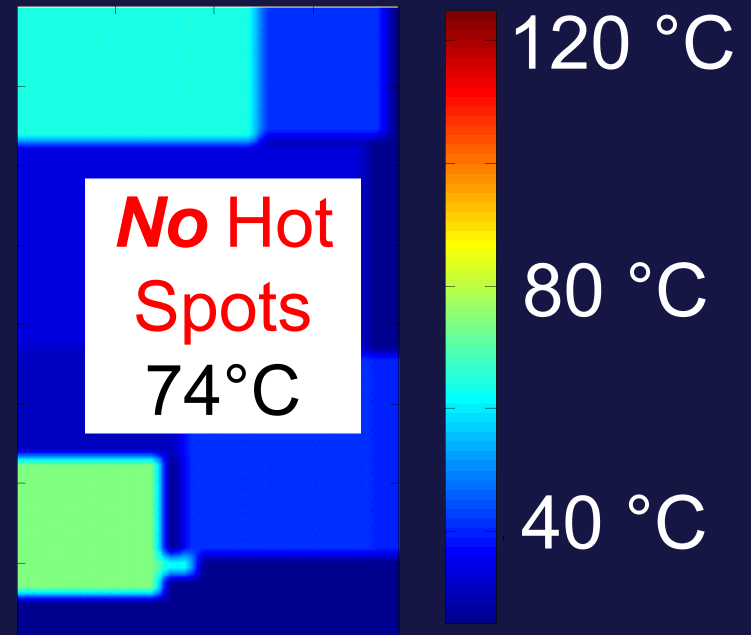


OpenSPARC T2 core-on-core

No PDN in model

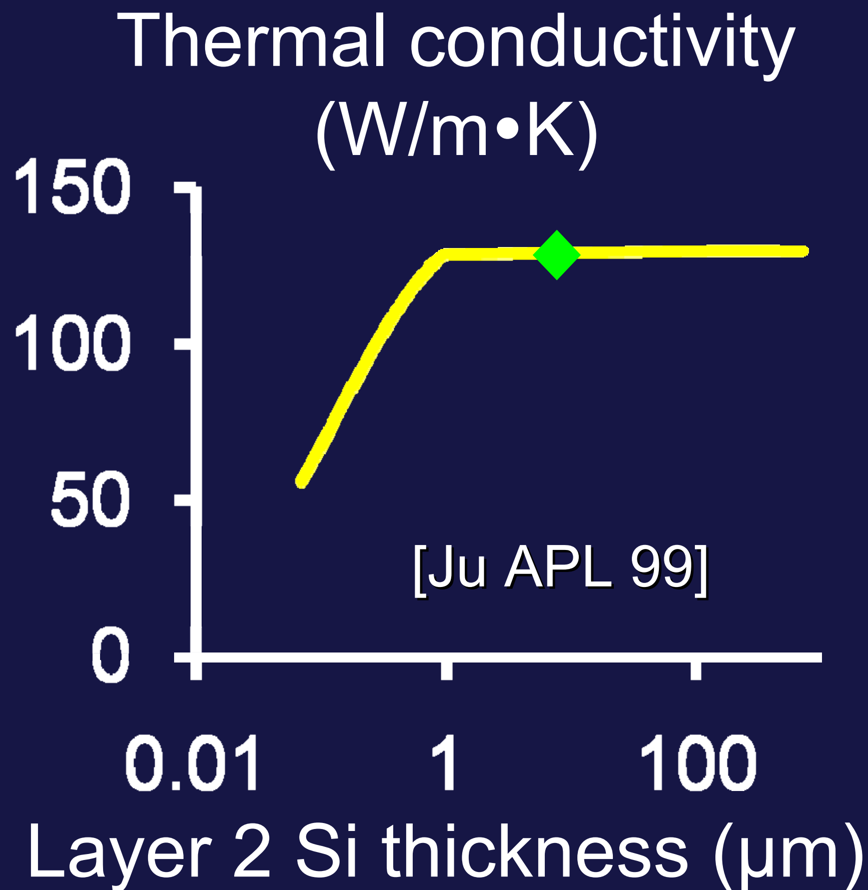
Thermal-aware PDN

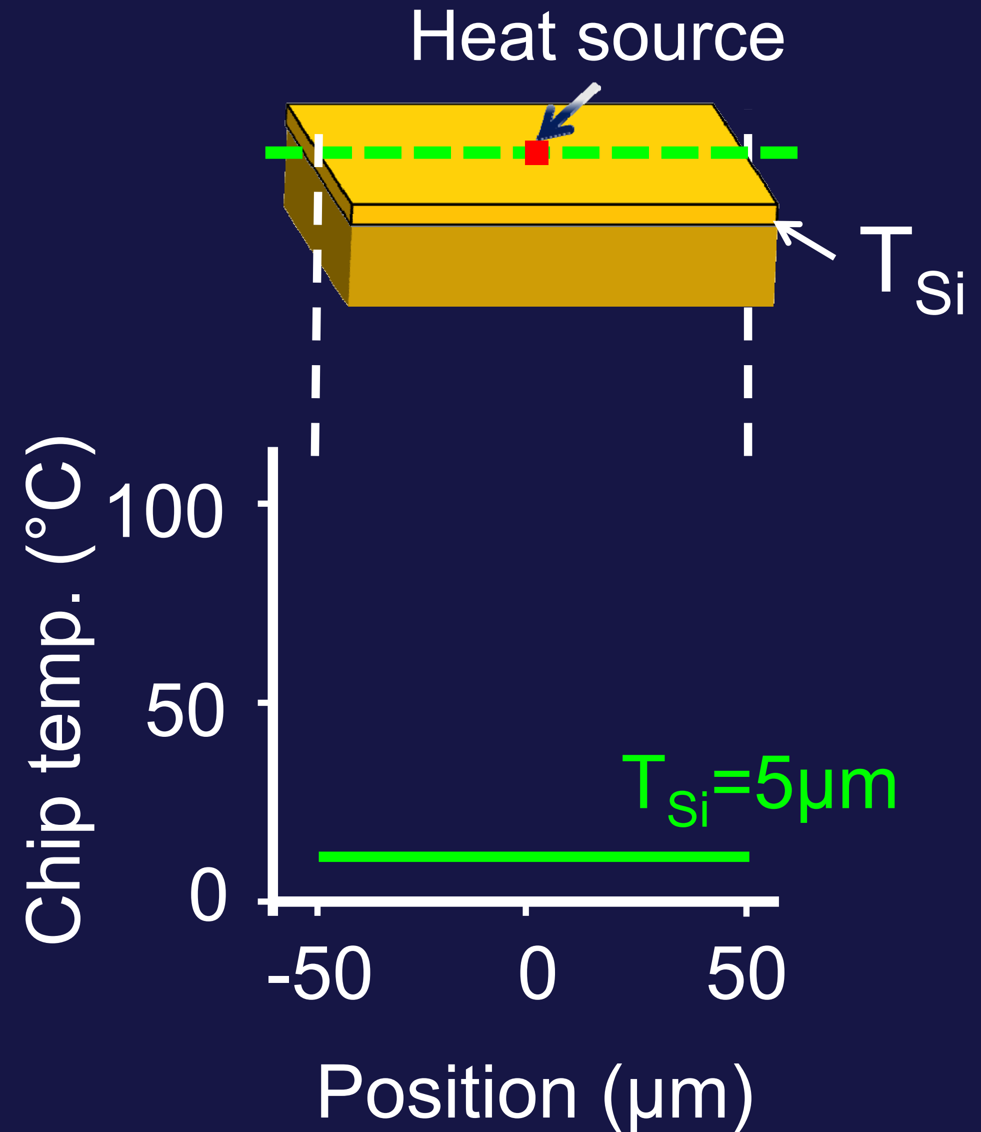




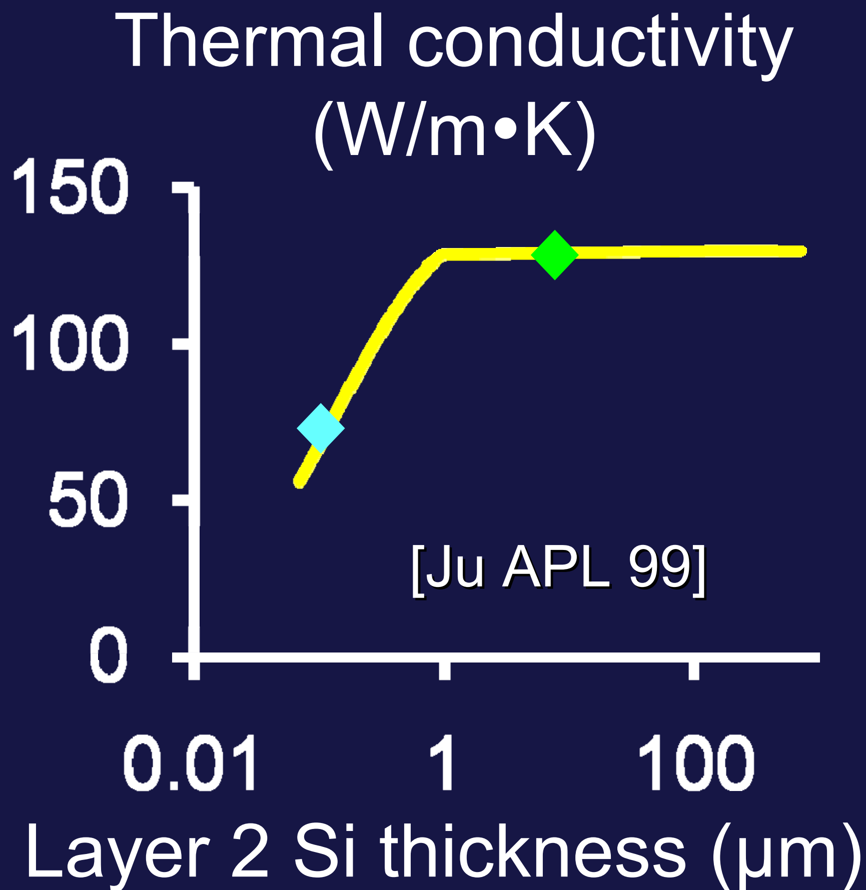
Layer 2 temperature map

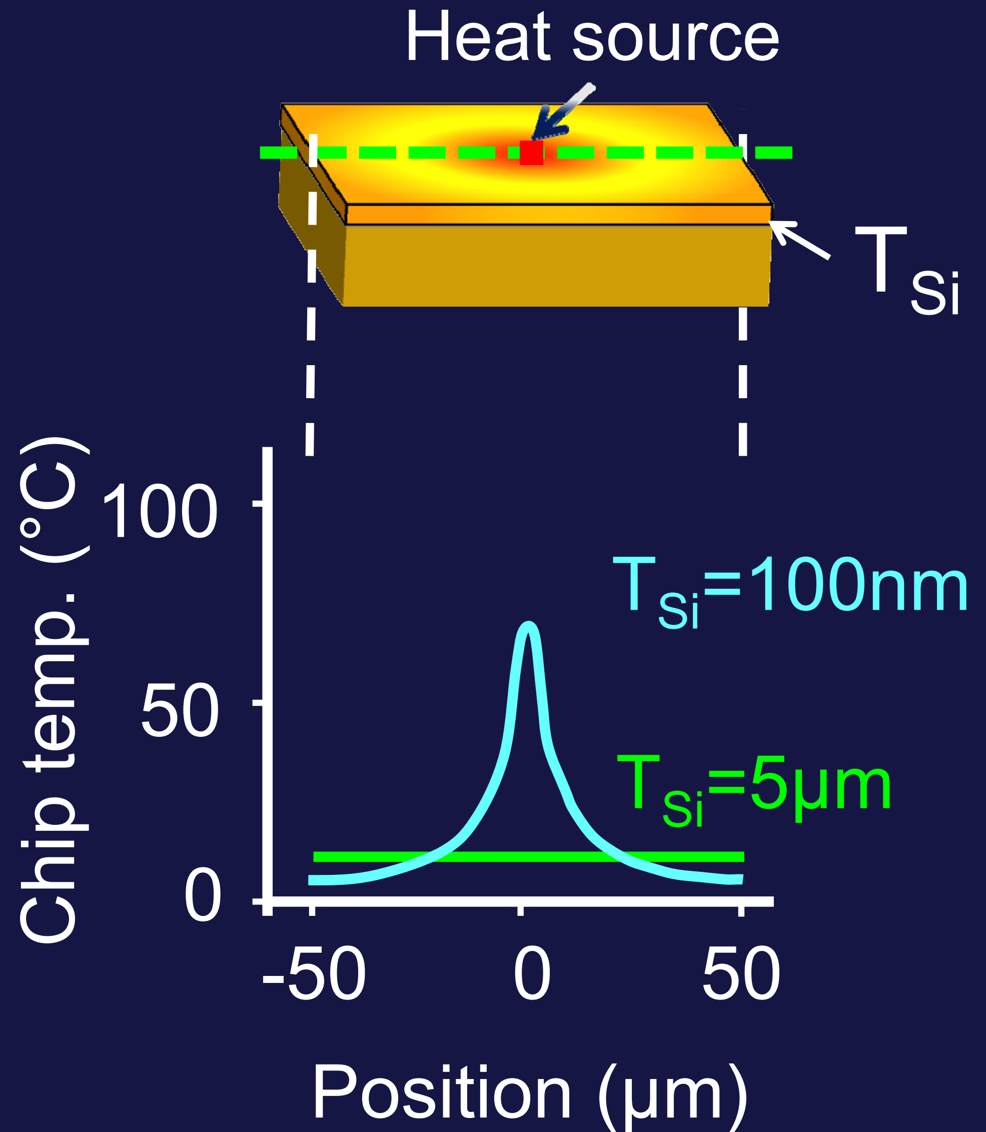
Lateral Conduction Challenge





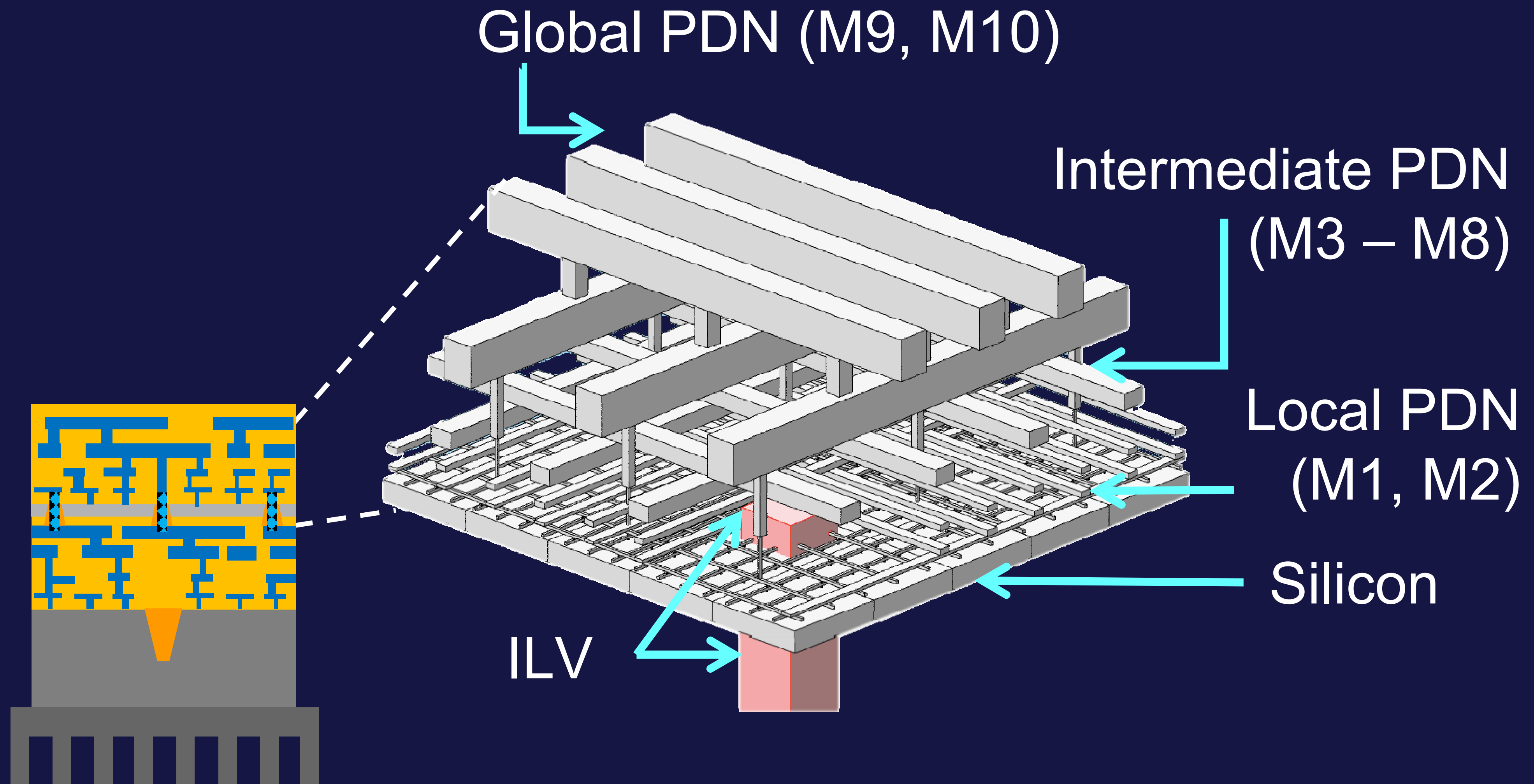
Lateral Conduction Challenge



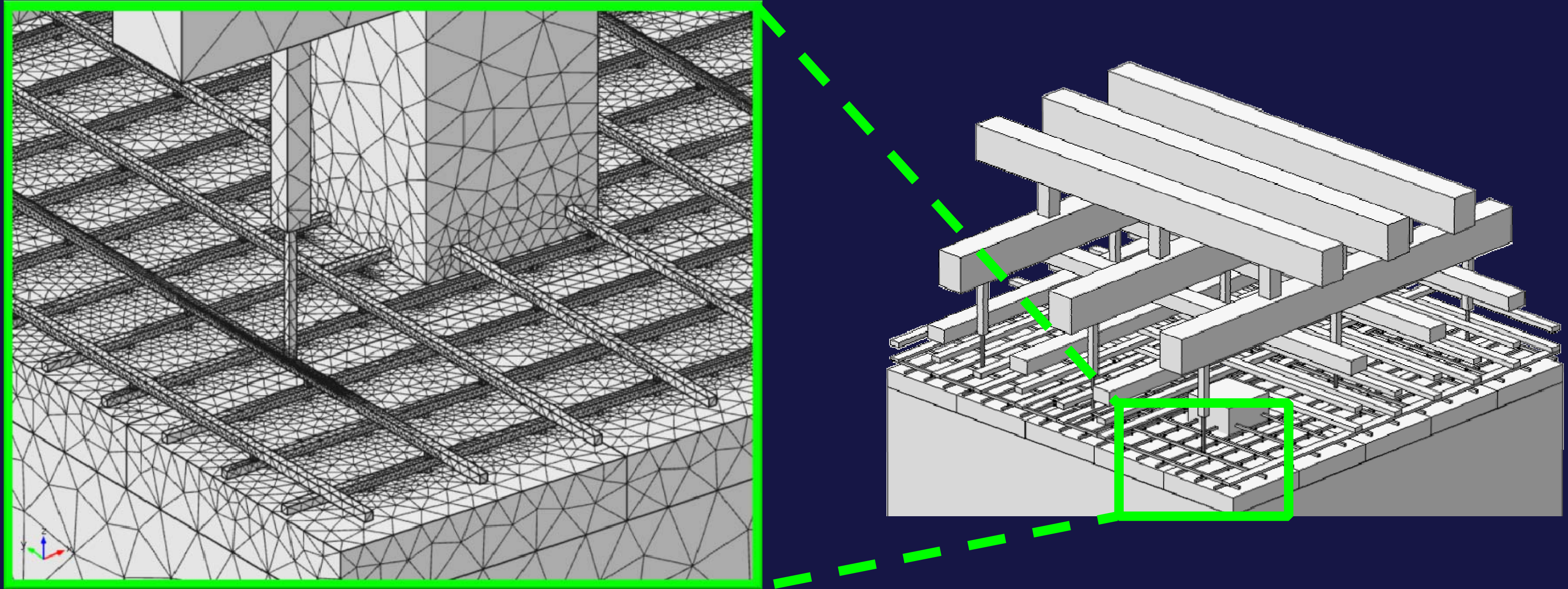


3 Grades of PDNs

- All copper



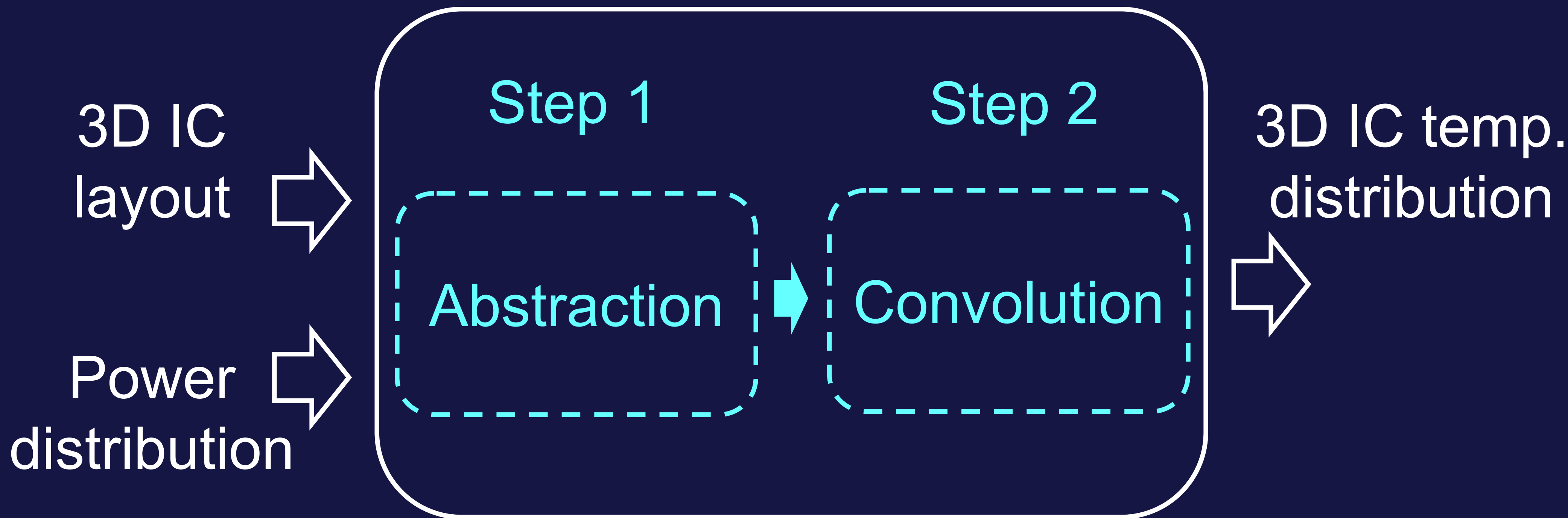
Finite Element Method



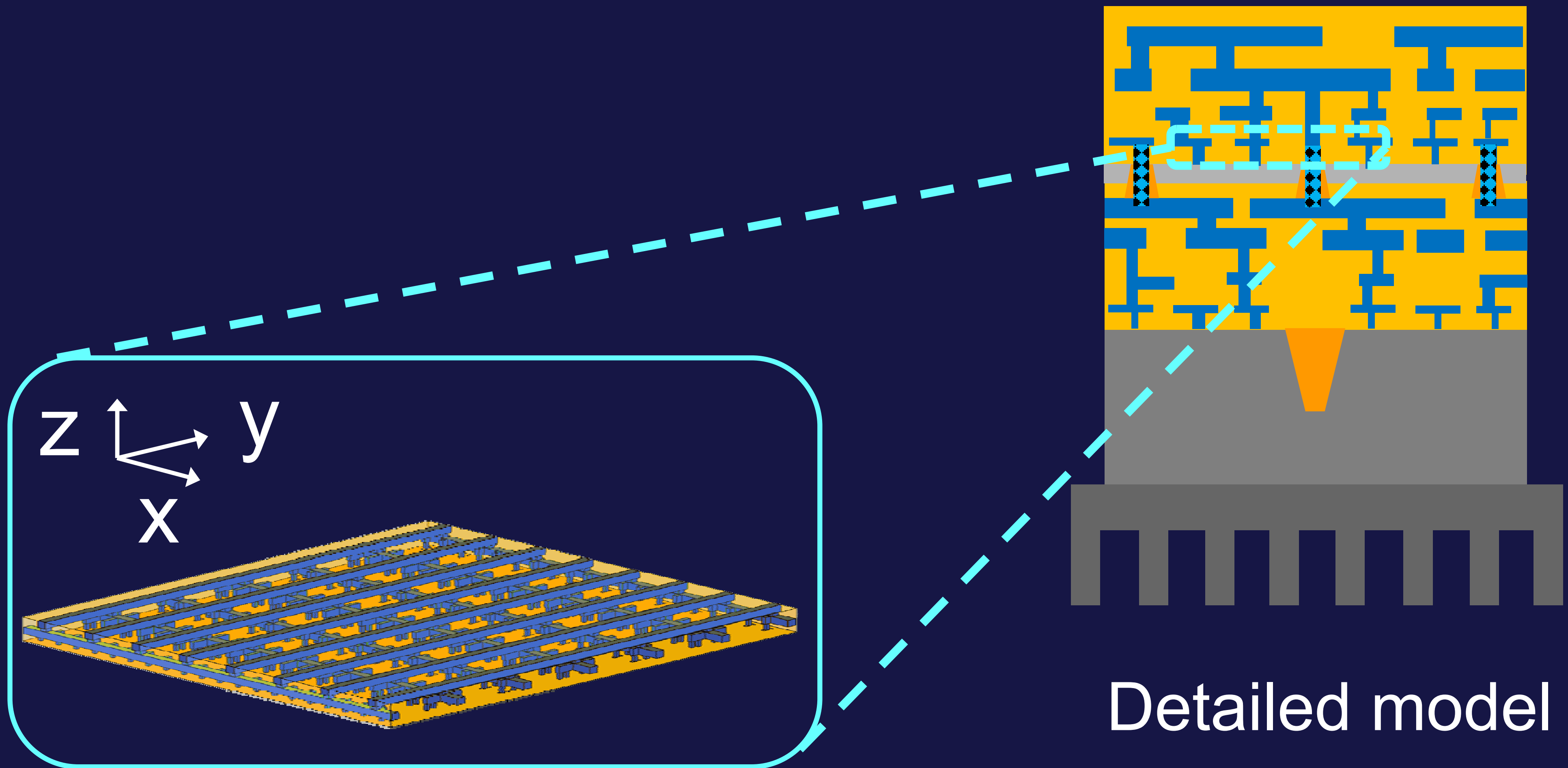
Comsol (25μm × 25μm block)
Does not complete

Our Analysis Methodology

Full chip thermal analysis



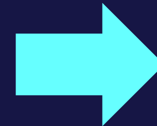
Step 1: Abstraction

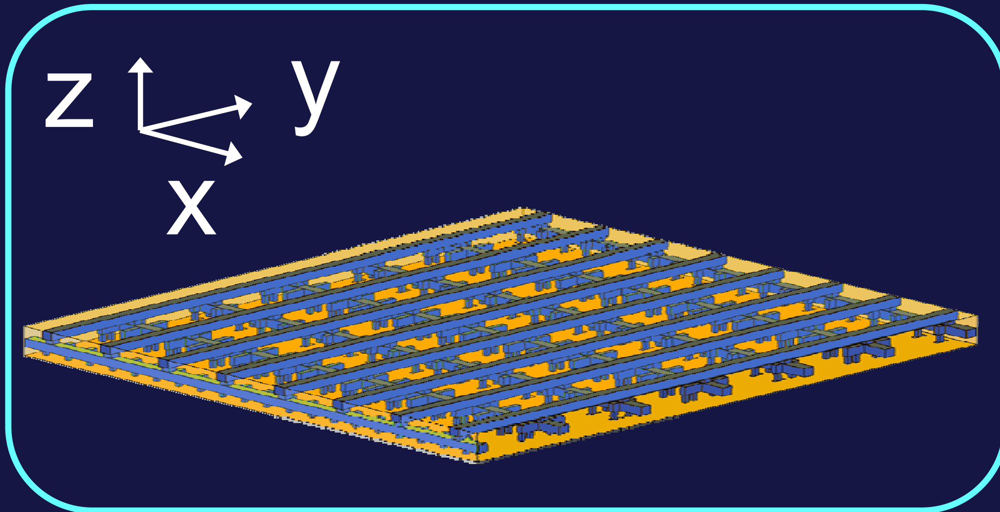


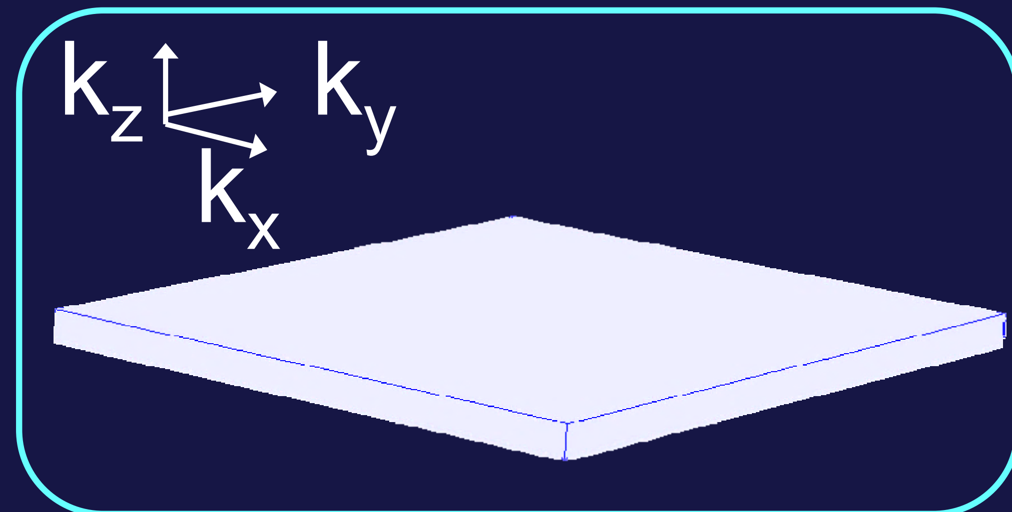
Detailed model

Step 1: Abstraction

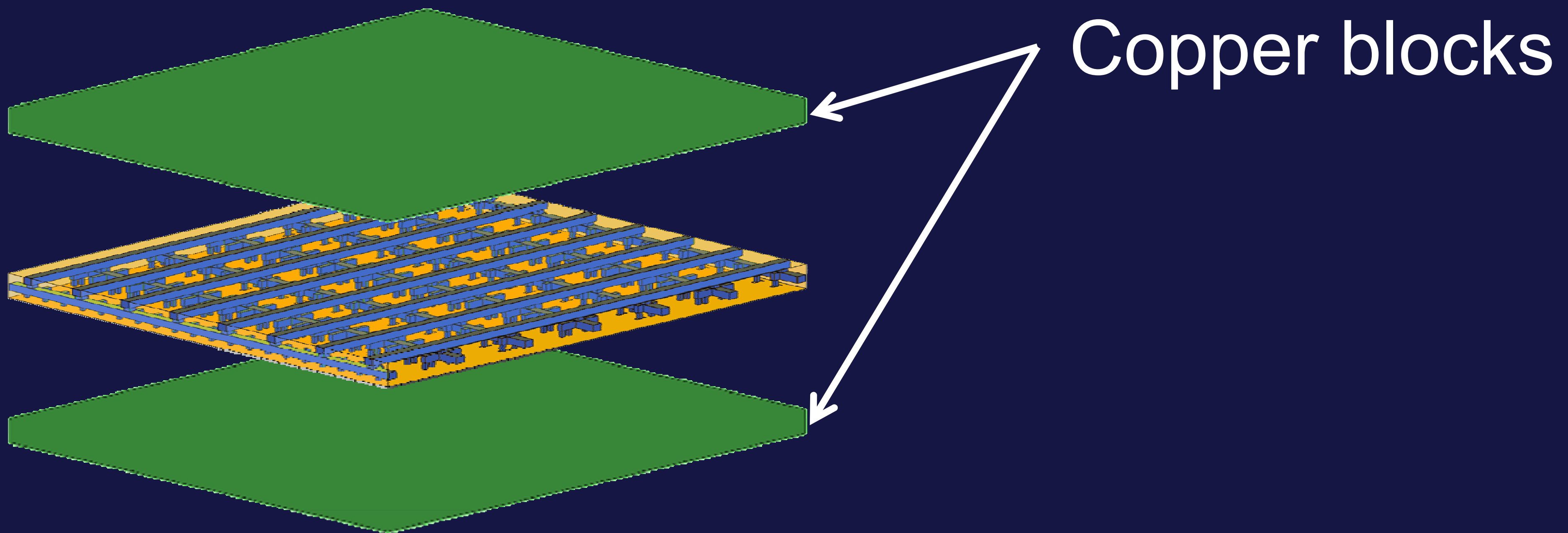
- k_z = Effective thermal conductivity in z direction

Detailed  Abstract

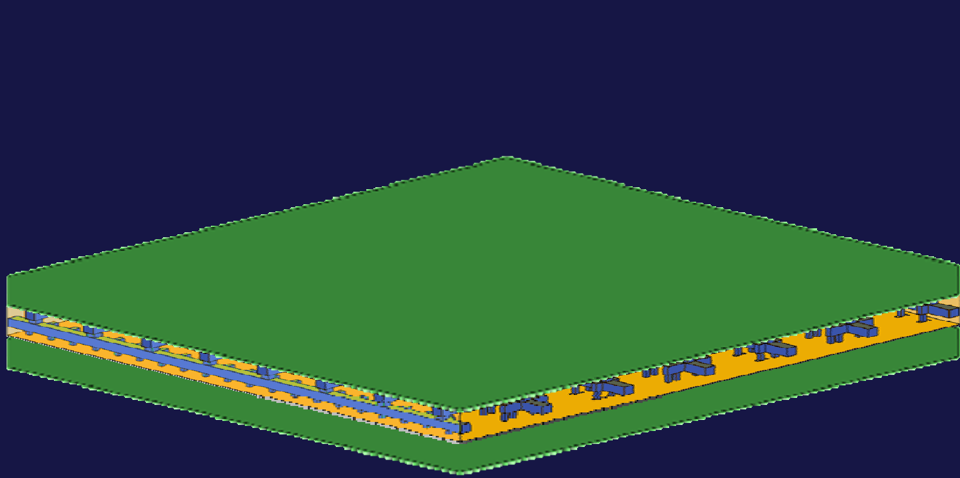




k_z Computation



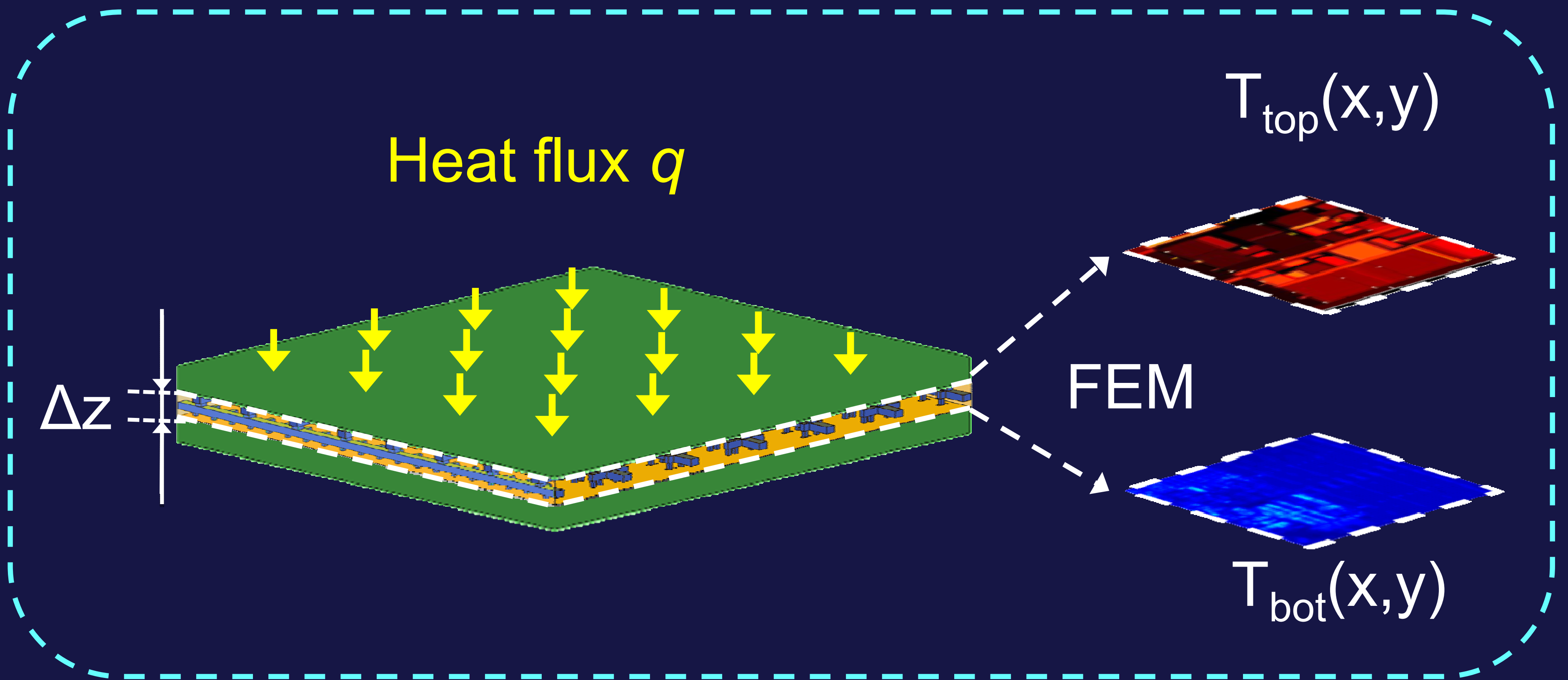
k_z Computation



k_z Computation

$$k_z = \frac{q \bullet \Delta z}{\overline{T_{top}} - \overline{T_{bot}}}$$

$\overline{X}$: mean of X



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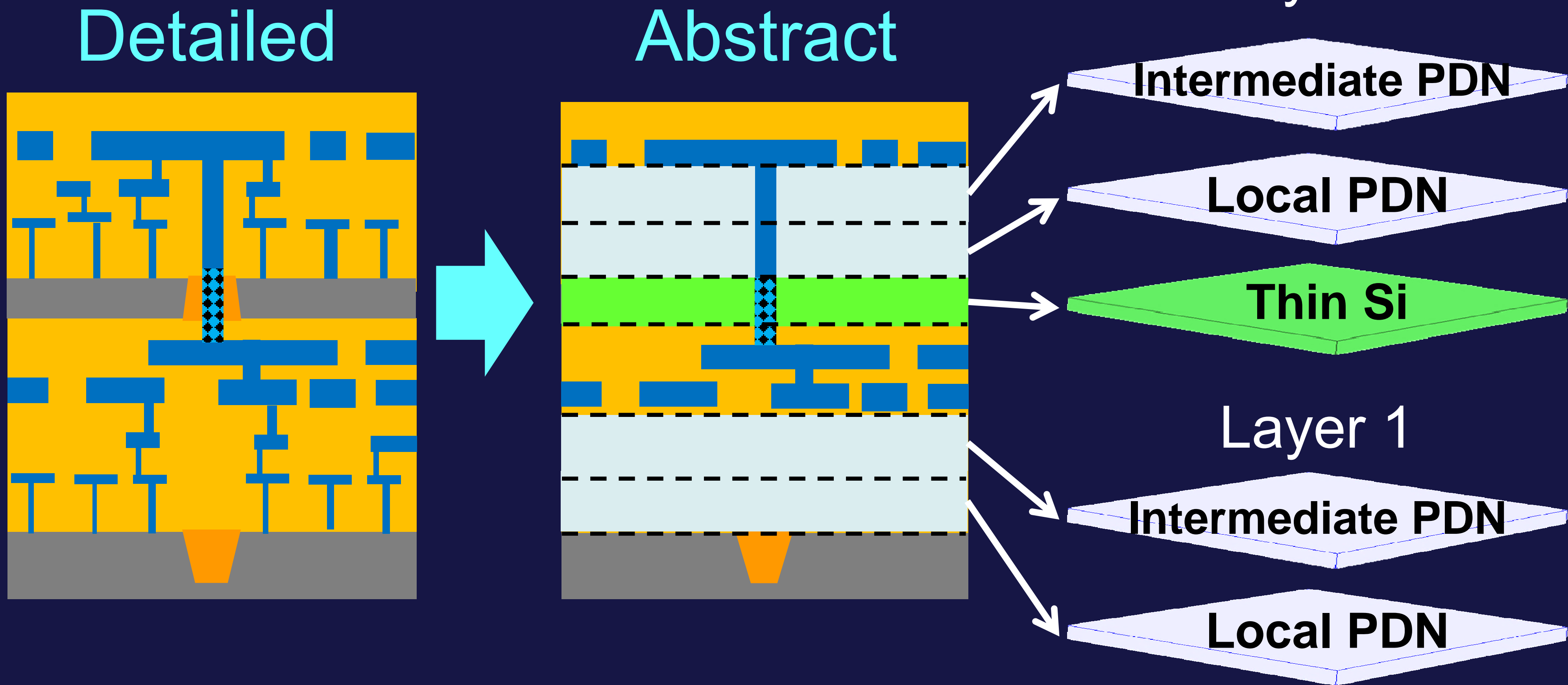
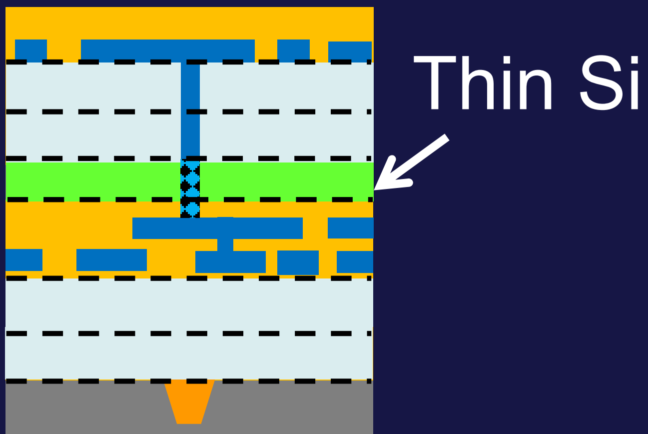


Step 2: Convolution

- 3D IC: linear system [Kemper THERMINIC 06]

Step 2: Convolution

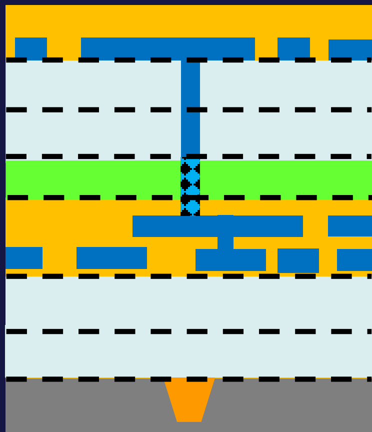
Abstract



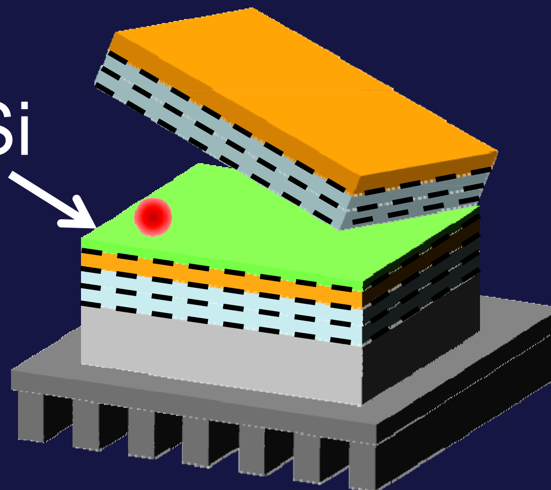
Step 2: Convolution

Abstract

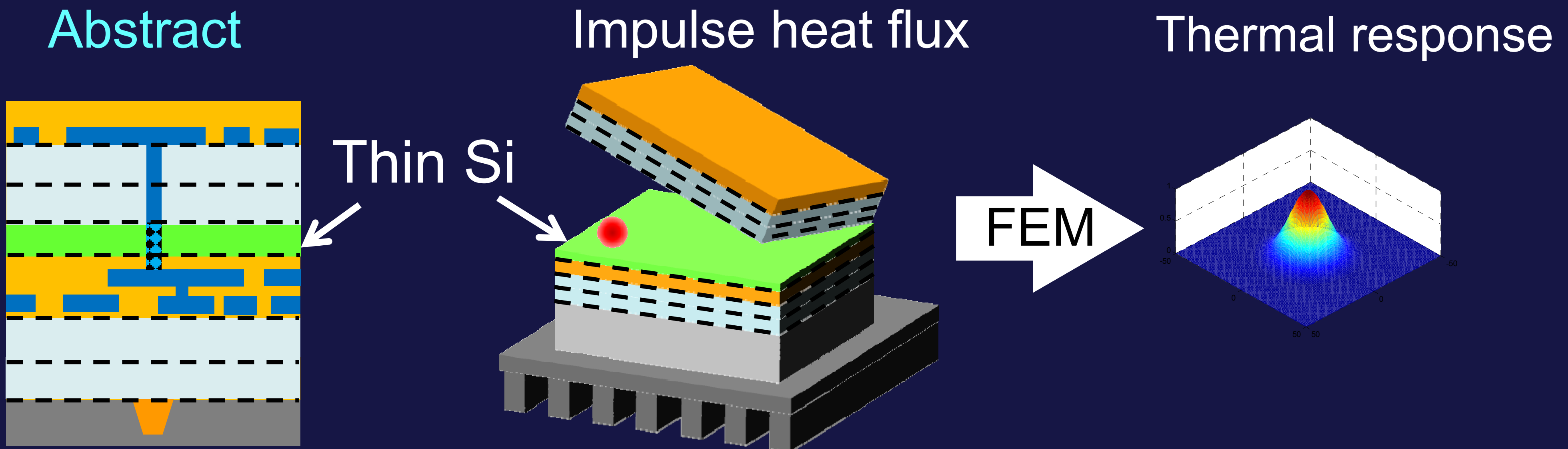
Impulse heat flux



Thin Si



Step 2: Convolution



Step 2: Convolution

Abstract

Impulse heat flux

Set of responses

Thin Si

FEM

Step 2: Convolution

Abstract

Impulse heat flux

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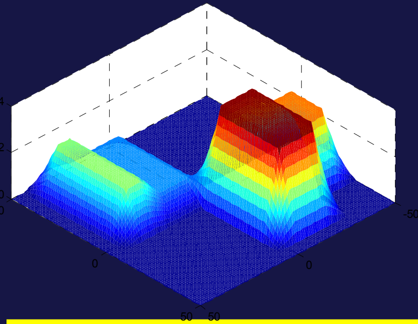


Power dissipation in thin Si layer
(Commercial tools)

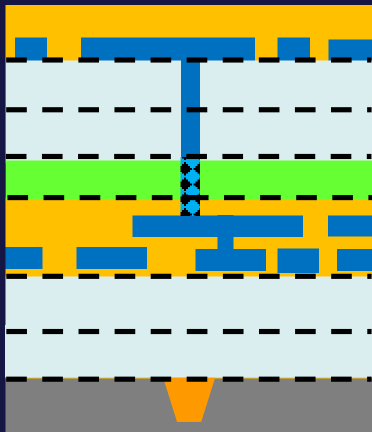
Power distribution

Impulse response

Convolution

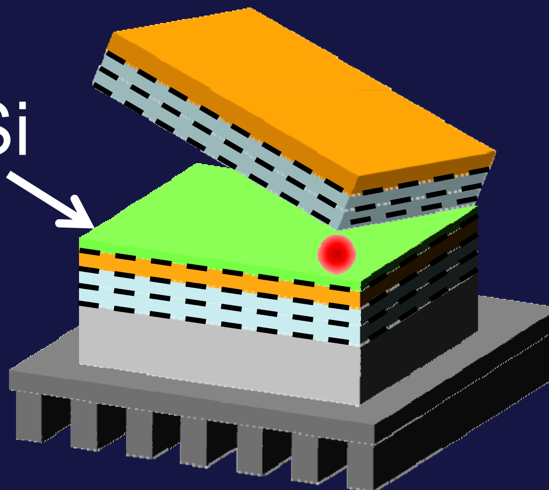
Temp. distribution

Abstract



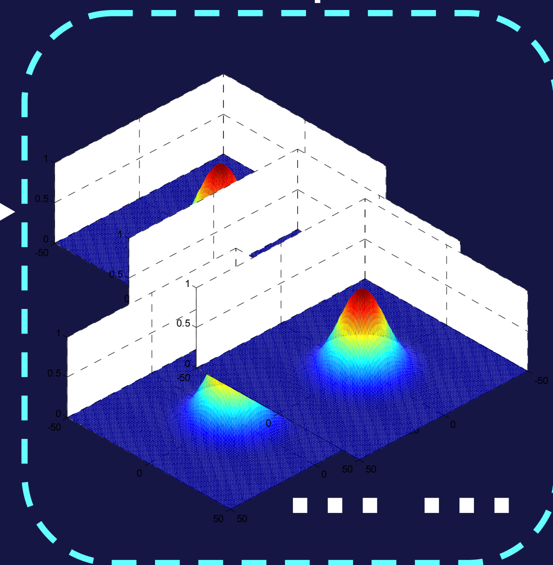
Thin Si

Impulse heat flux

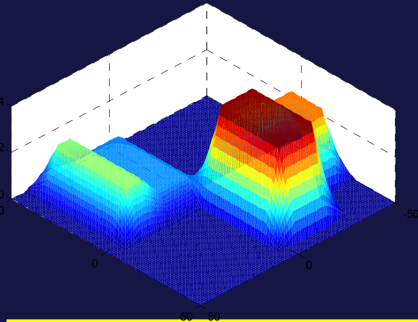


FEM

Set of responses



Step 2: Convolution



Power dissipation in thin Si layer
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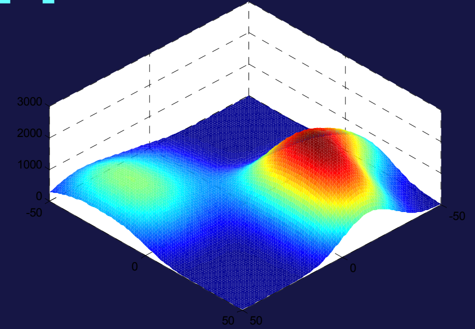


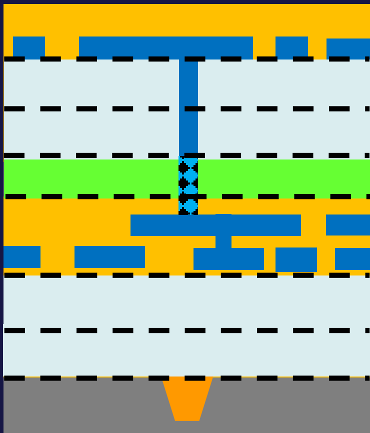
Power distribution

Impulse response

Convolution

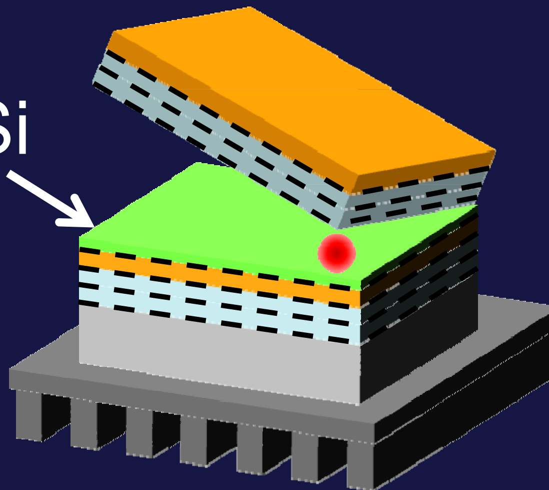
Temp. distribution

Abstract



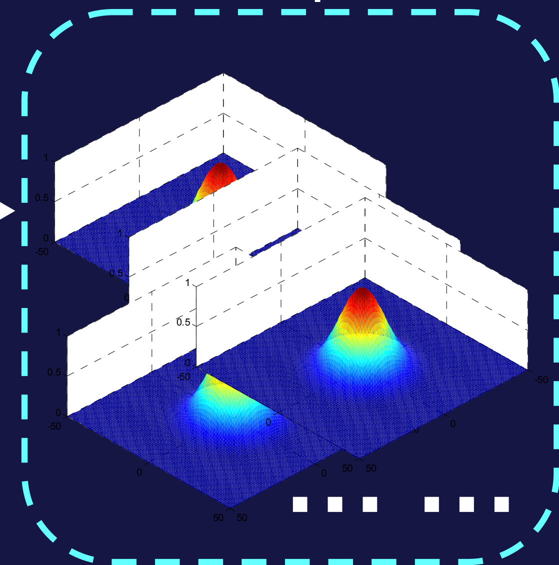
Thin Si

Impulse heat flux

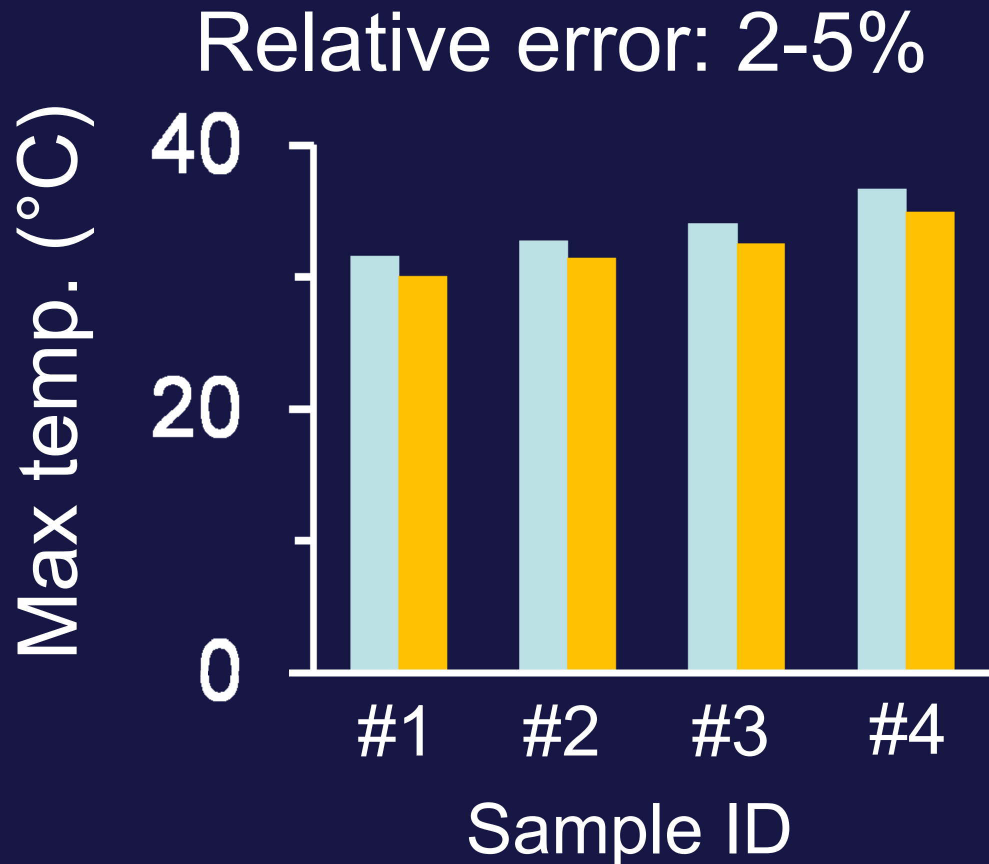


FEM

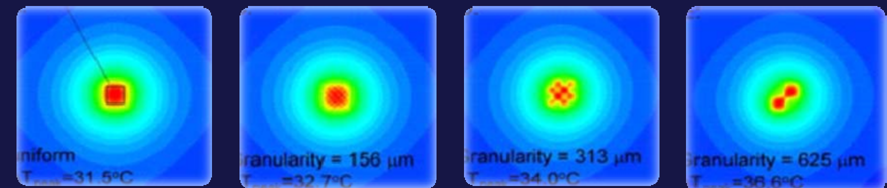
Set of responses



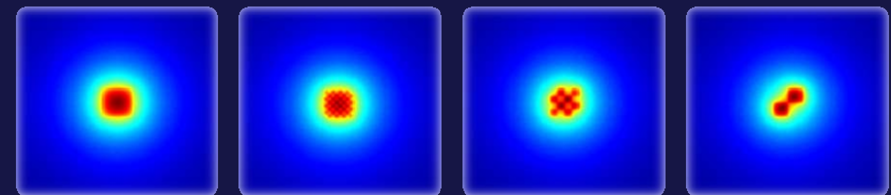
Model Verification



Published results
[Etessam-Yazdani ICPES 06]



Our results



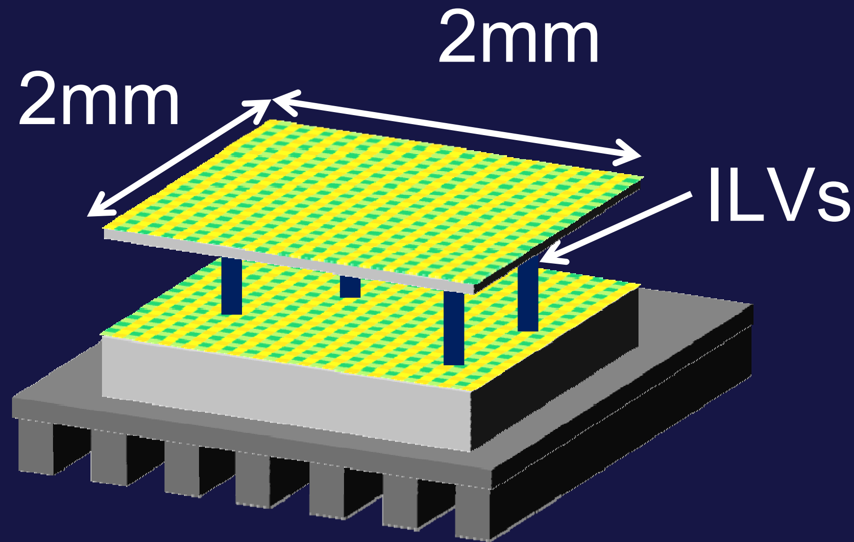
#1 #2 #3 #4

Sample ID

■ Published results ■ Our results

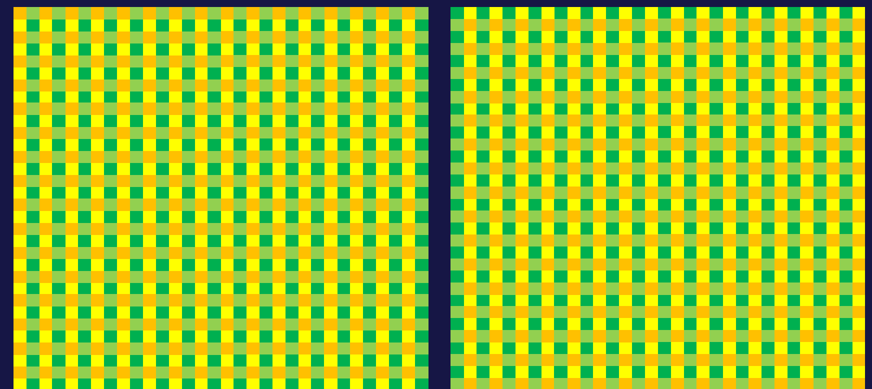
Thermal Analysis: Example 1

- Average: 50 W/cm^2 per layer



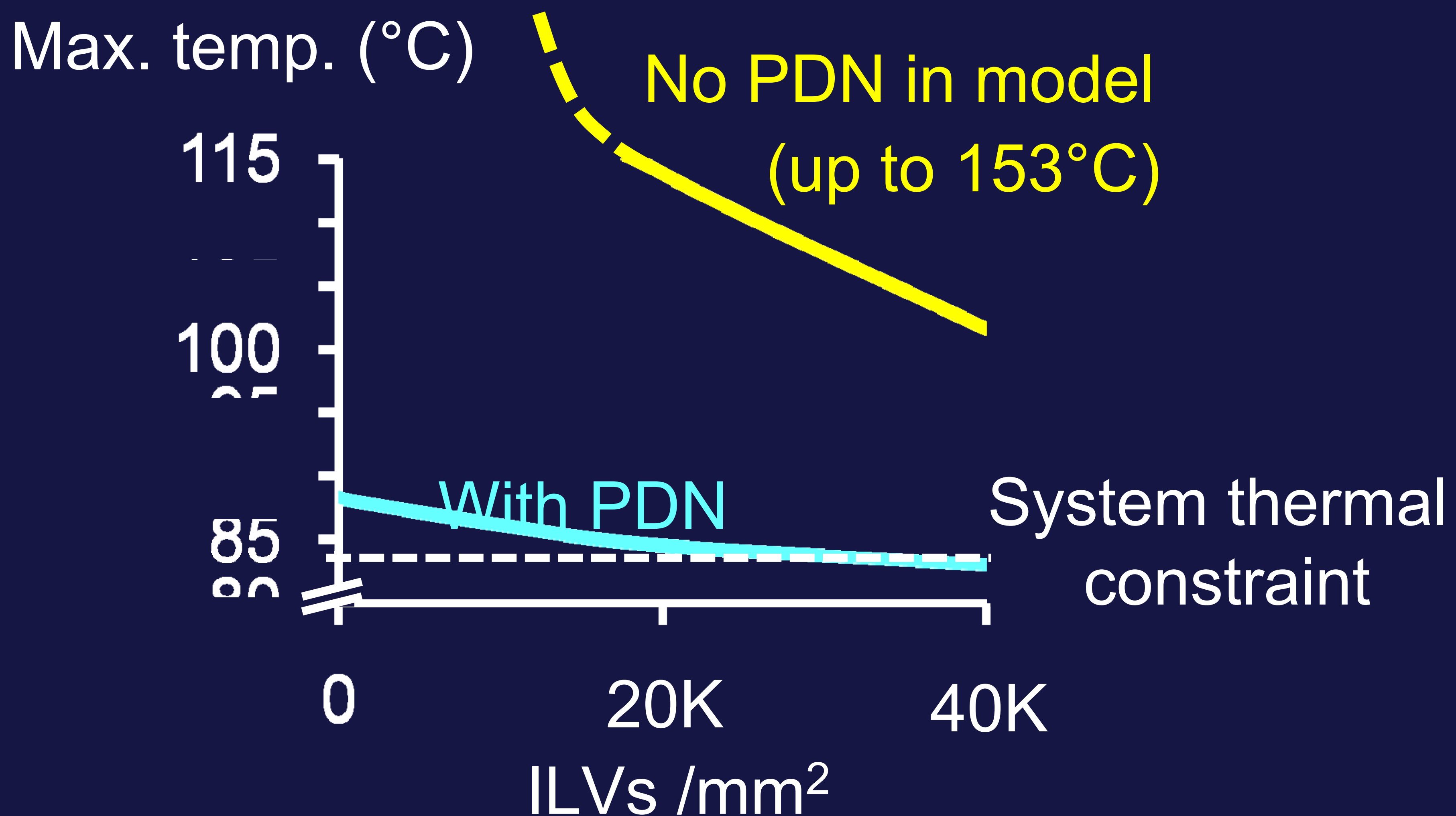
Air cooling: 2 $W/K \cdot cm^2$

Power distribution map



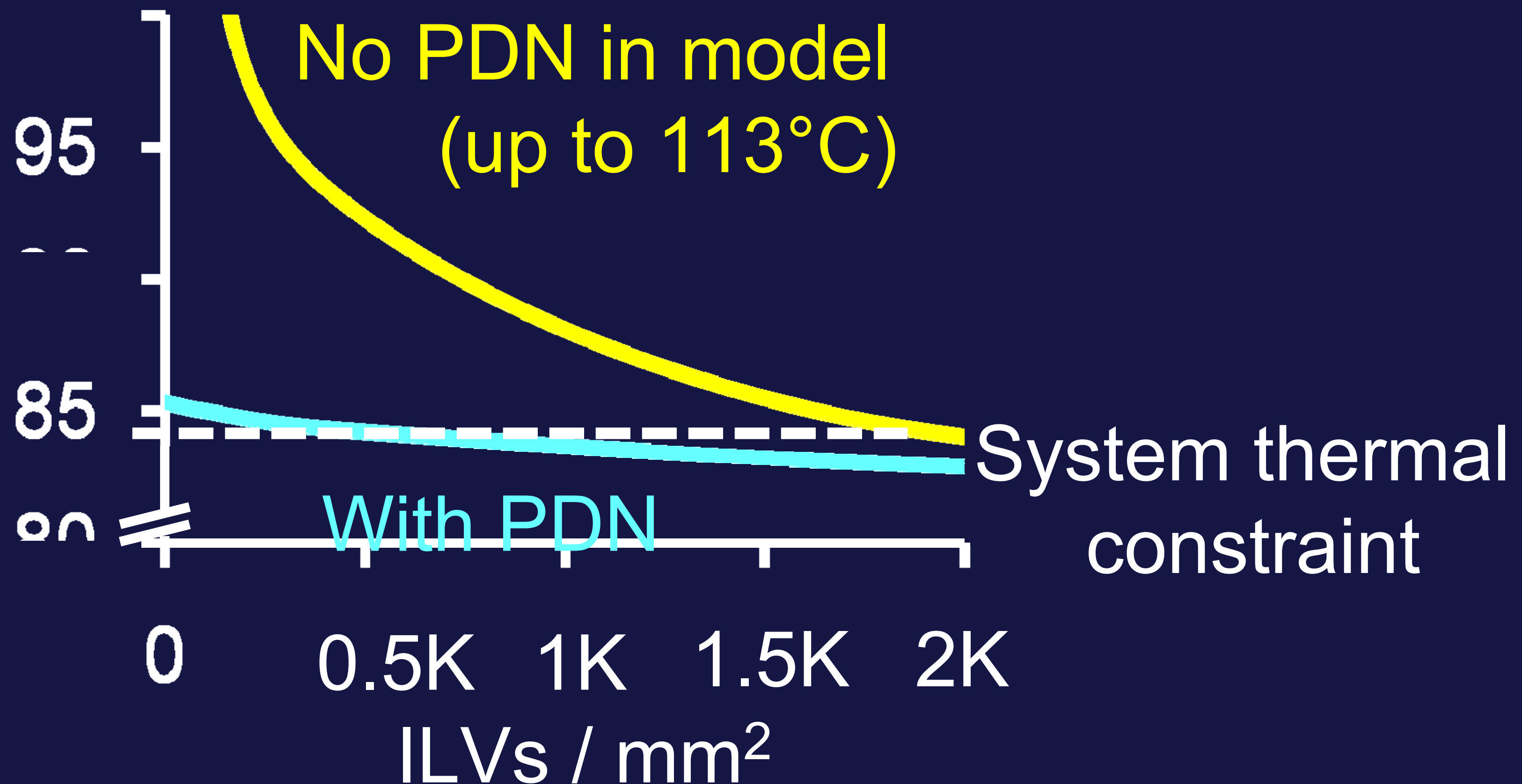
Example 1 Results

- Monolithic 3D IC: big temperature benefit



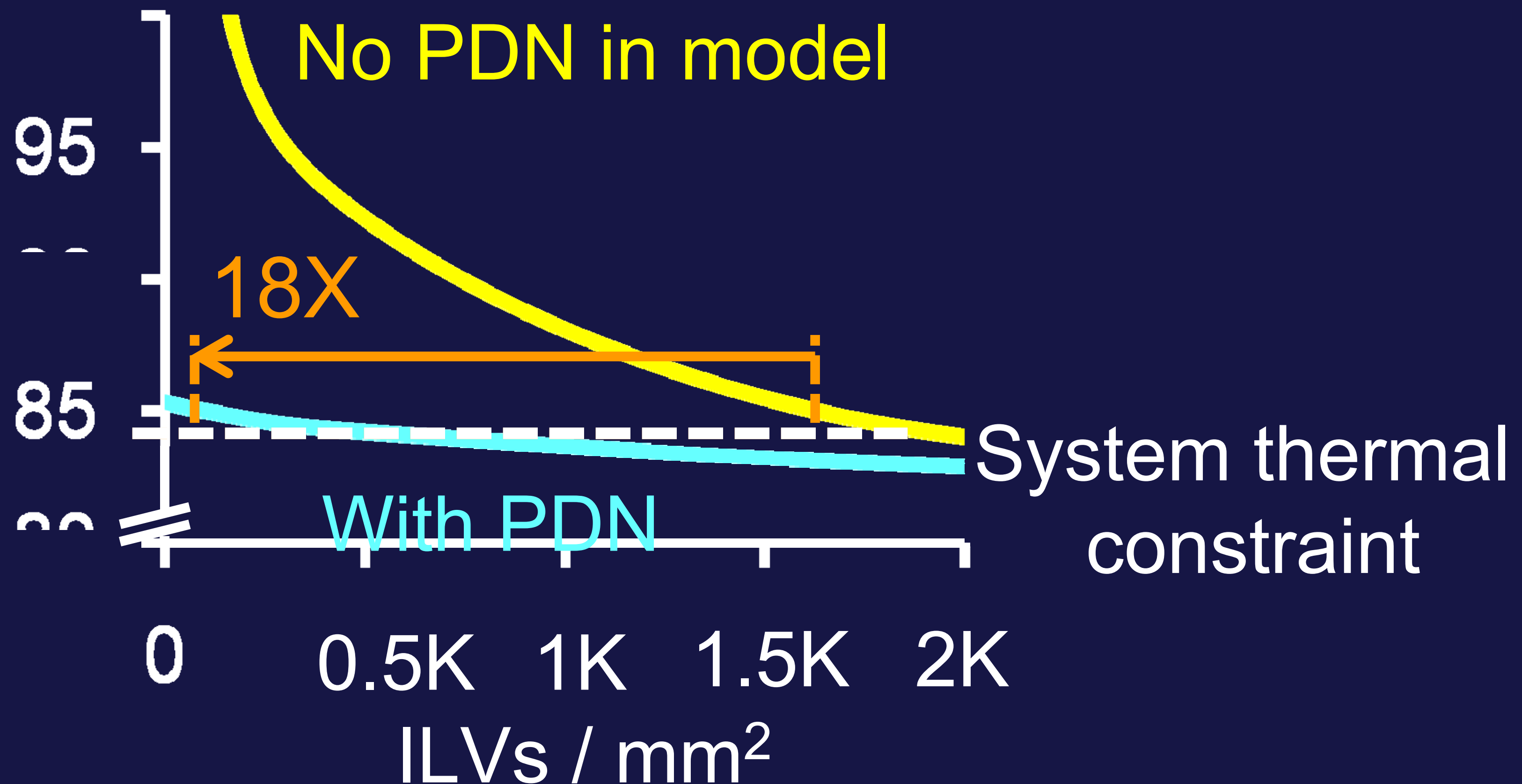
Example 1 Results

- Parallel 3D IC: area benefit



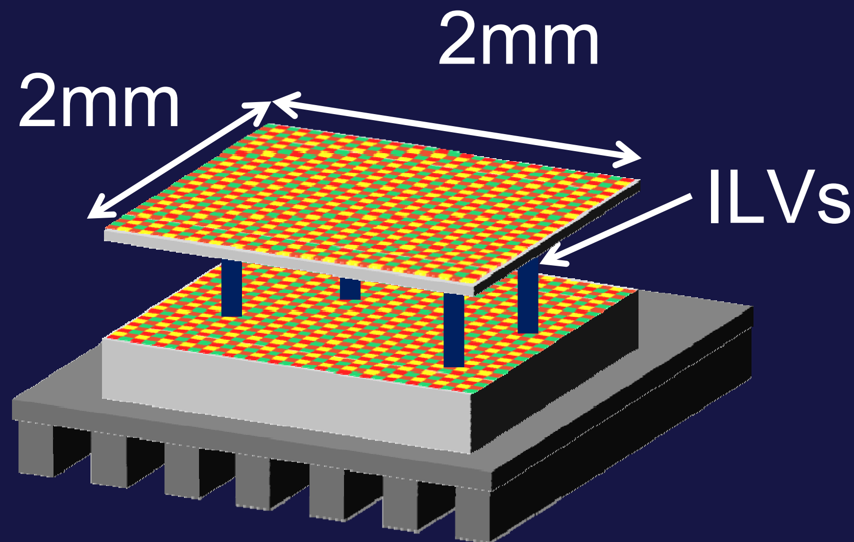
Example 1 Results

- Parallel 3D IC: area benefit



Thermal Analysis: Example 2

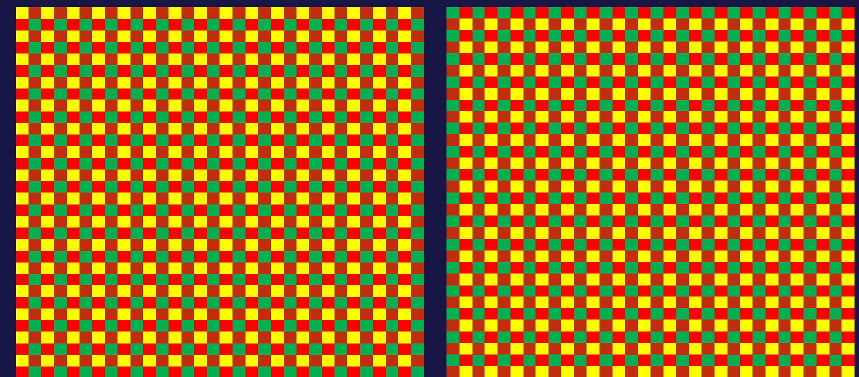
- Average: 125 W/cm^2 per layer



Air cooling: 2 $W/K \cdot cm^2$

Temp. drop on heat sink: 125°C

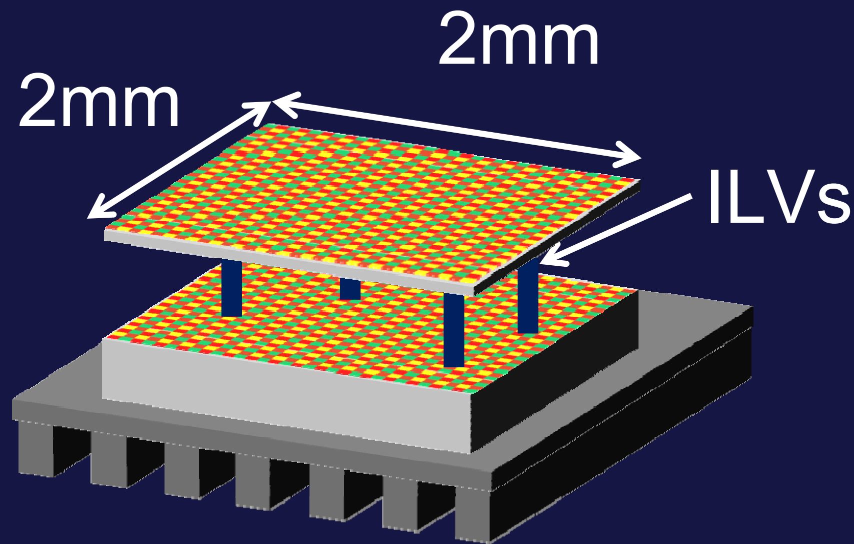
Power distribution map



Power density (W/cm^2)

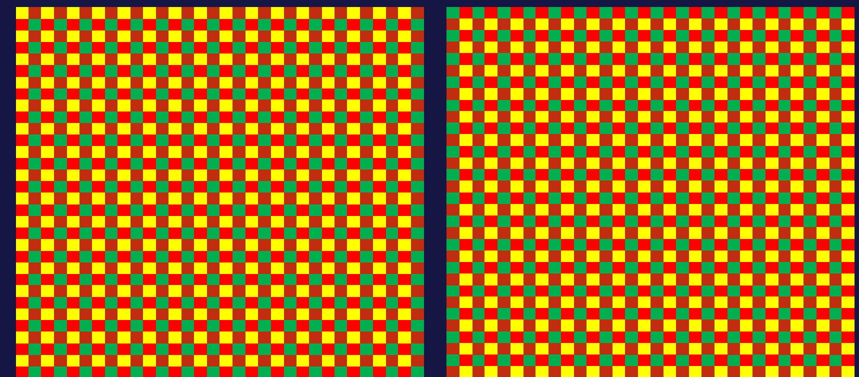
Thermal Analysis: Example 2

- Average: 125 W/cm^2 per layer



Power distribution map

Layer 1 Layer 2

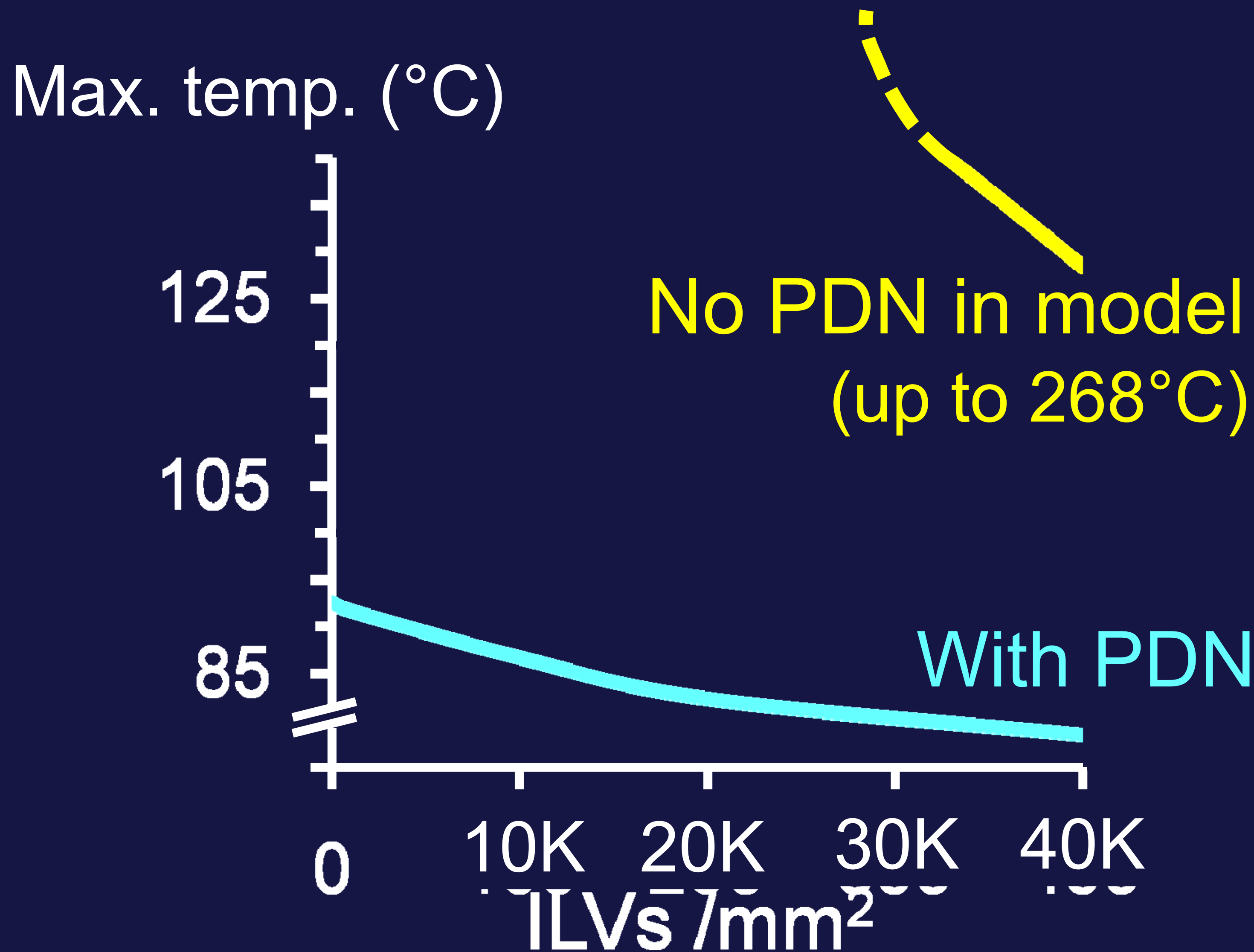


External liquid cooling: 10 $W/K \cdot cm^2$

Temp. drop on heat sink: 25°C

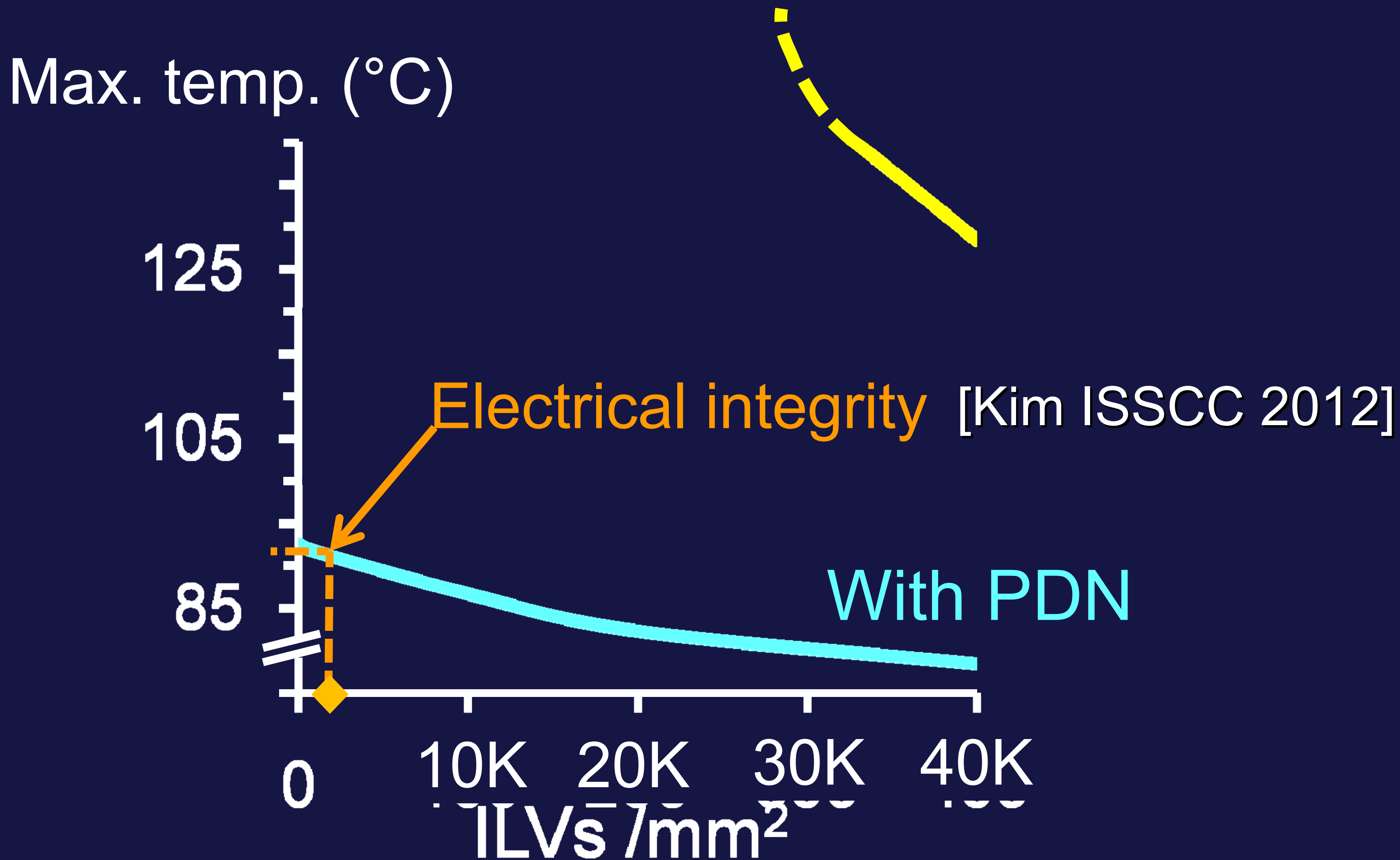
Example 2 Results

- Monolithic 3D IC: significant temperature benefit



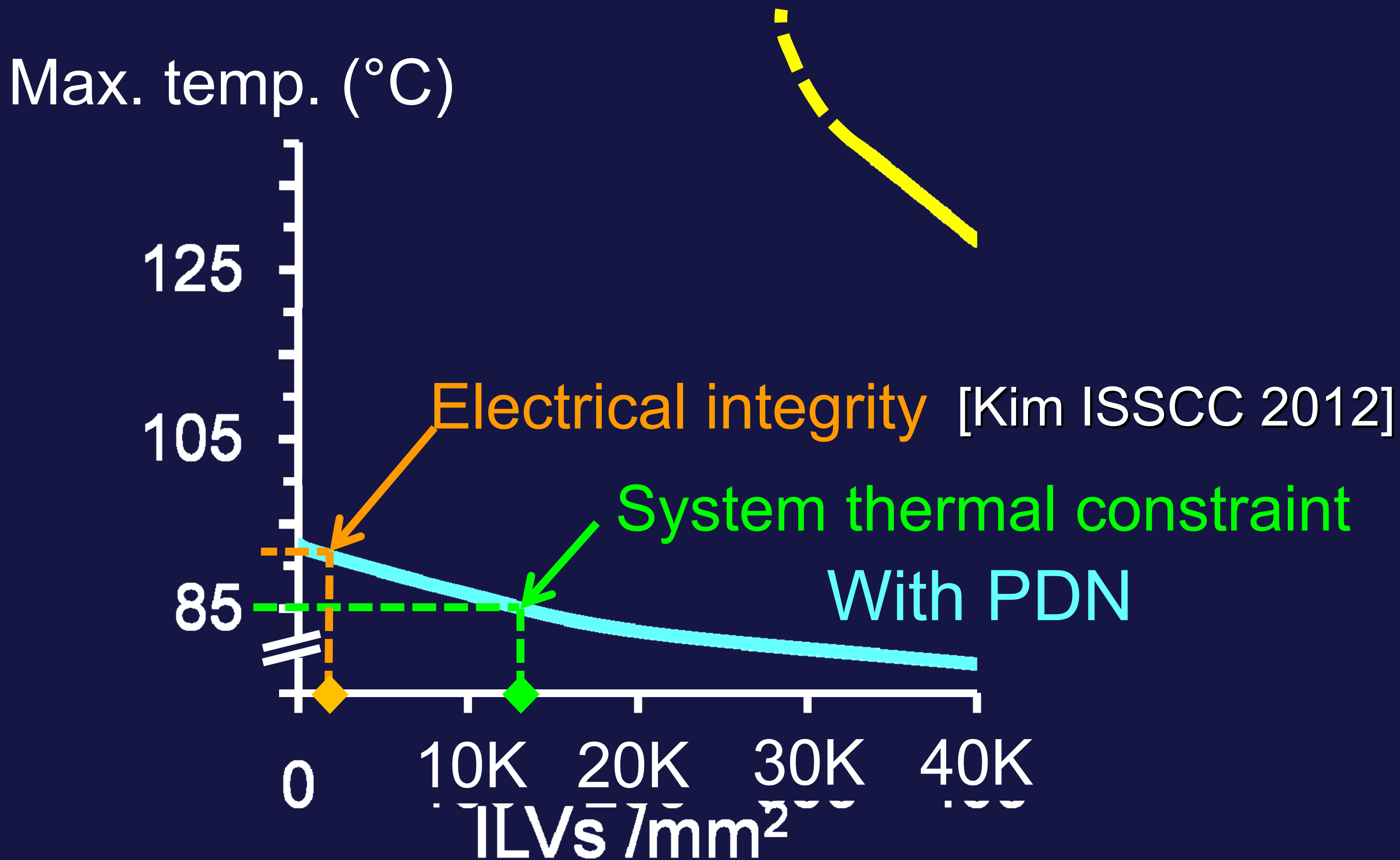
Thermal-Aware PDN

- Thermal-aware ILV density selection



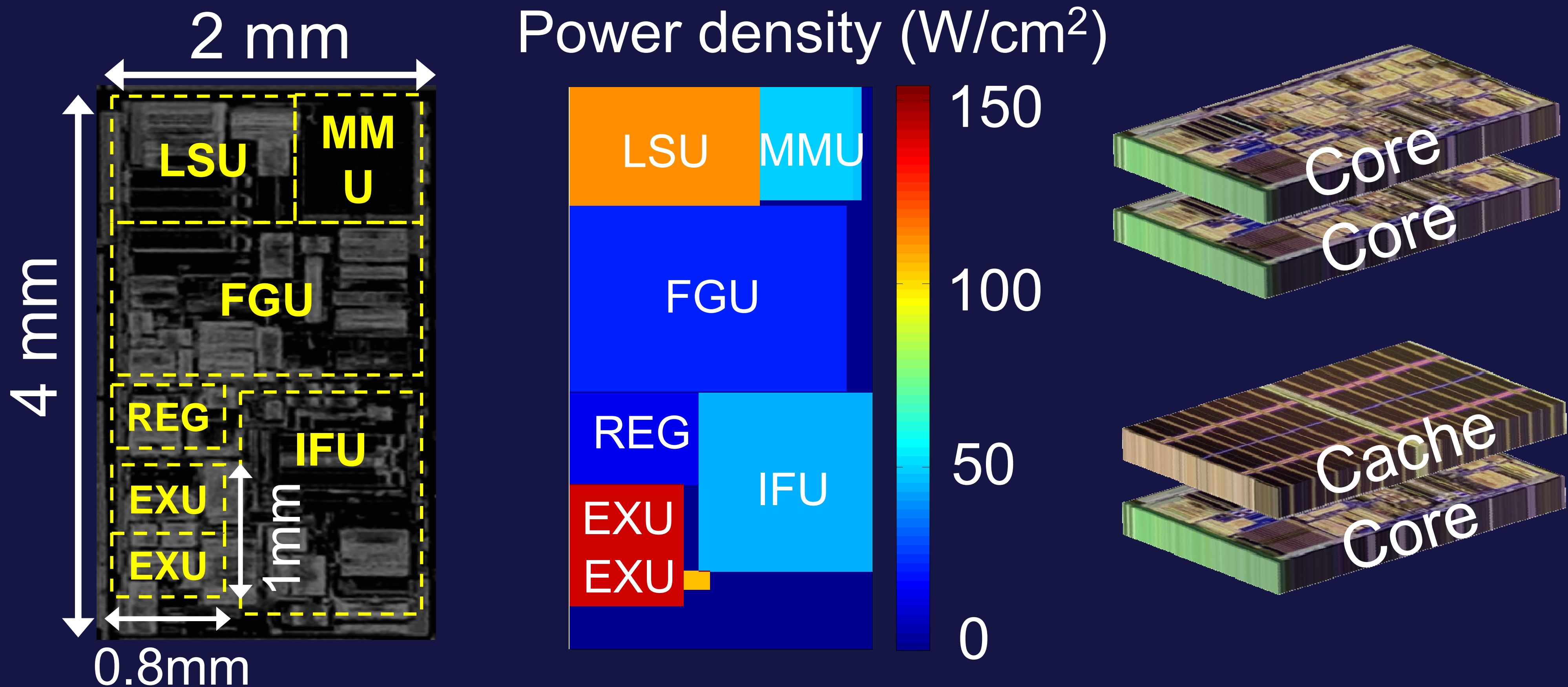
Thermal-Aware PDN

- Thermal-aware ILV density selection



OpenSPARC T2 Core

- Industrial design: 45nm
- Power distribution for Black-Scholes application



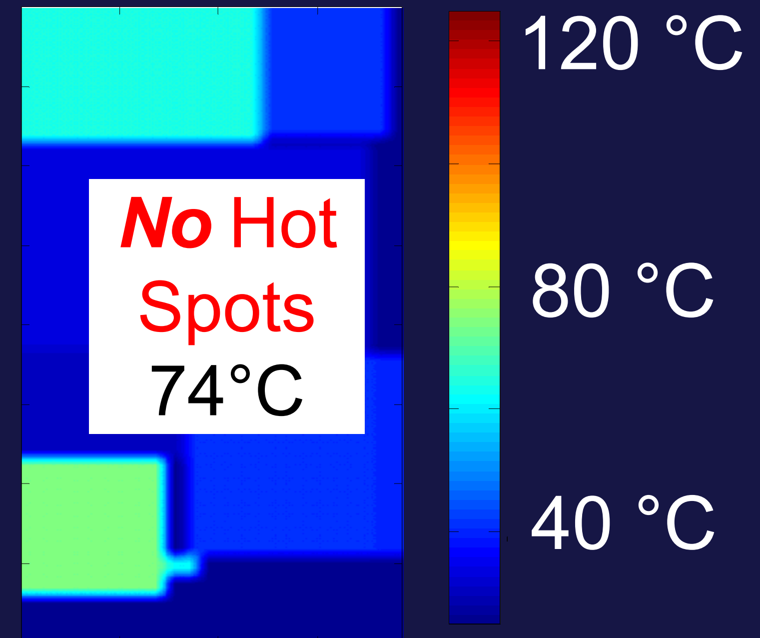
Core-on-Core Stacking

- Significant temperature benefit

Layer 2 temperature distribution

No PDN in model

Thermal-aware PDN



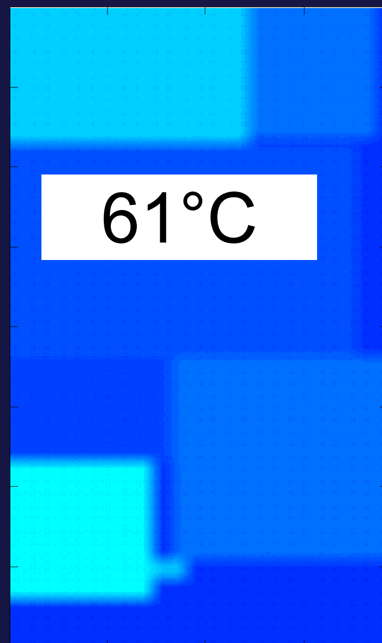
ILV density 10K ILVs/mm^2

Cache-on-Core Stacking

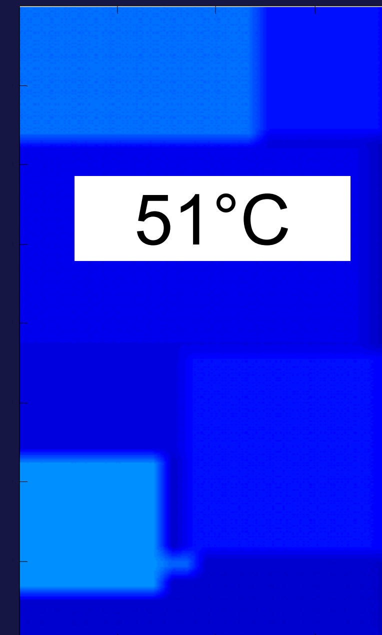
- Further temperature reduction

Layer 2 temperature distribution

No PDN in model



Thermal-aware PDN



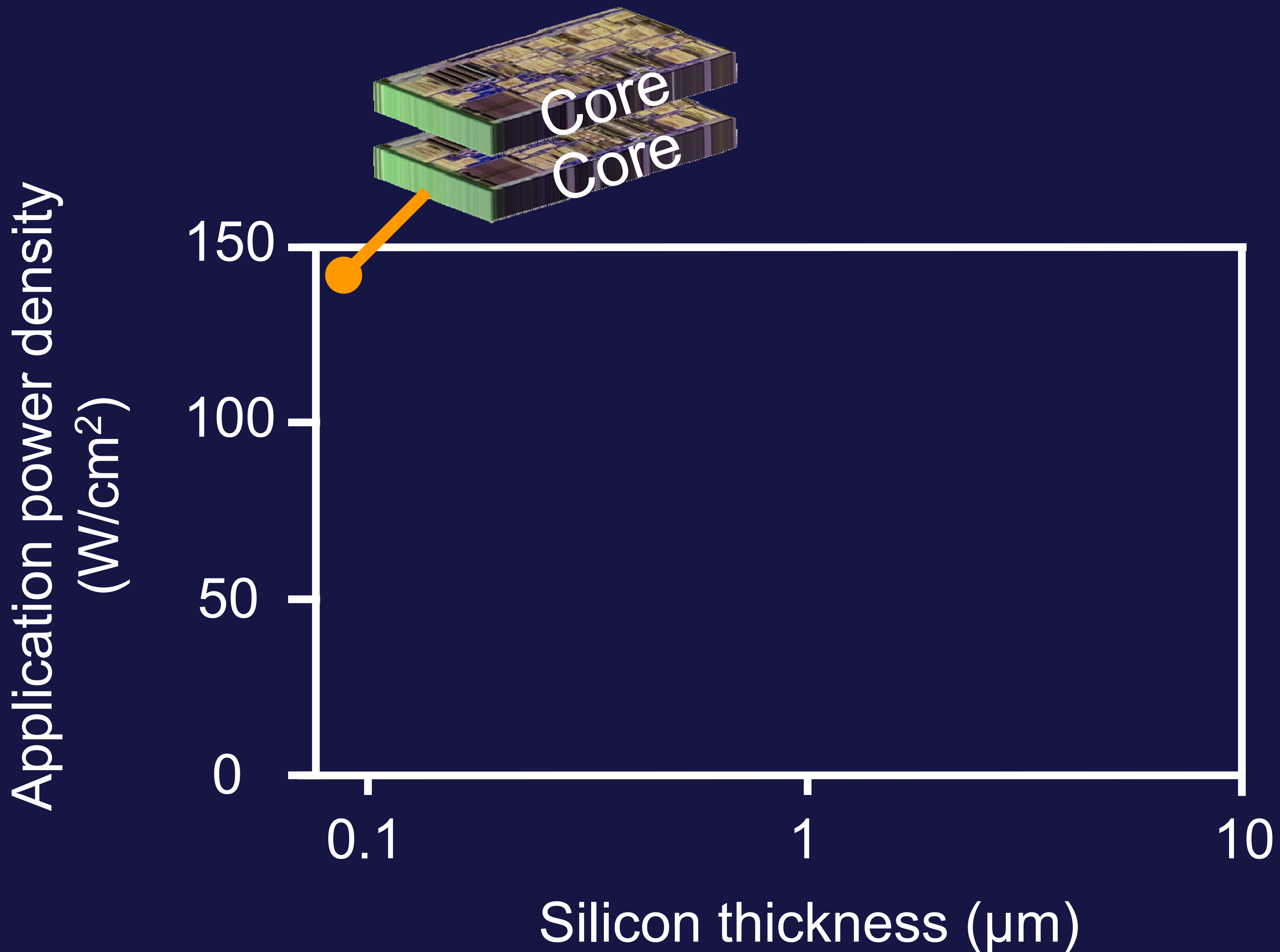
120 °C

80 °C

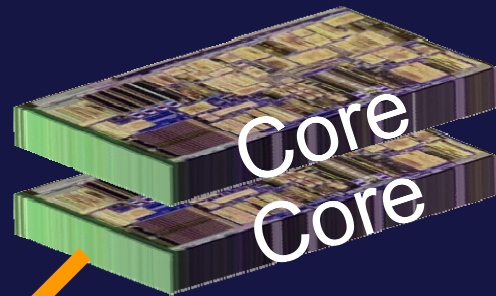
40 °C

ILV density 10K ILVs/mm^2

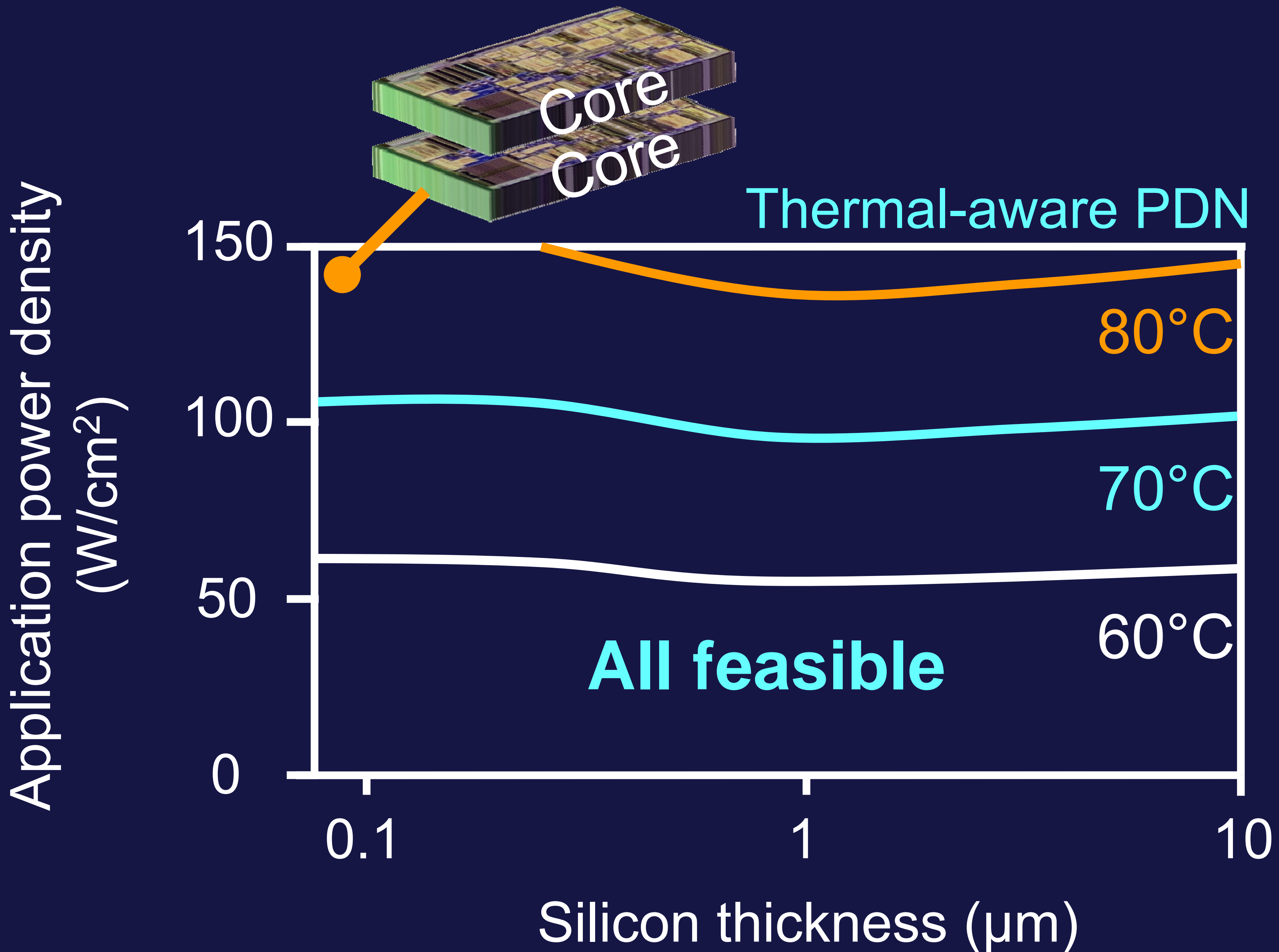
Technology vs. Application



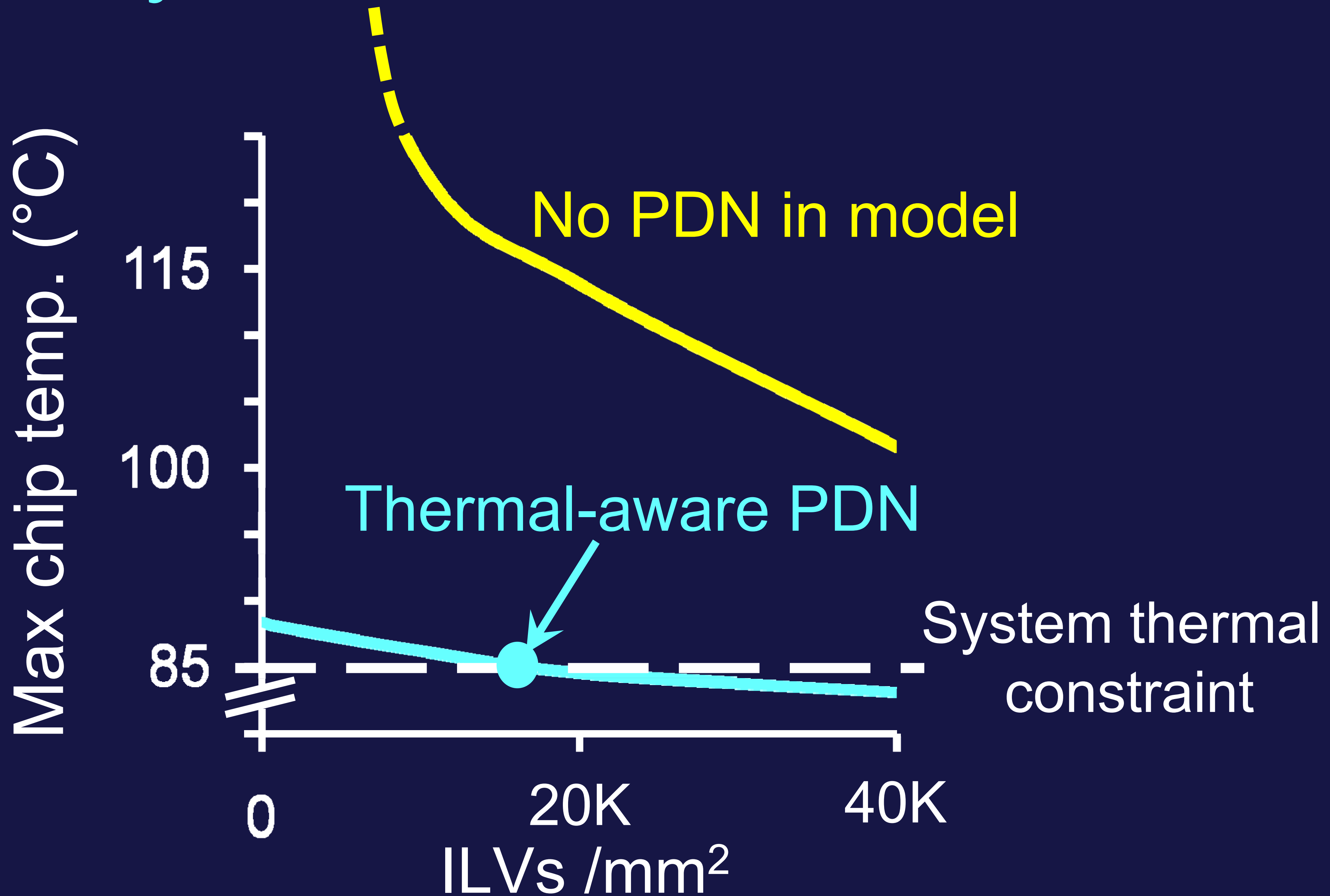
Technology vs. Application



Technology vs. Application



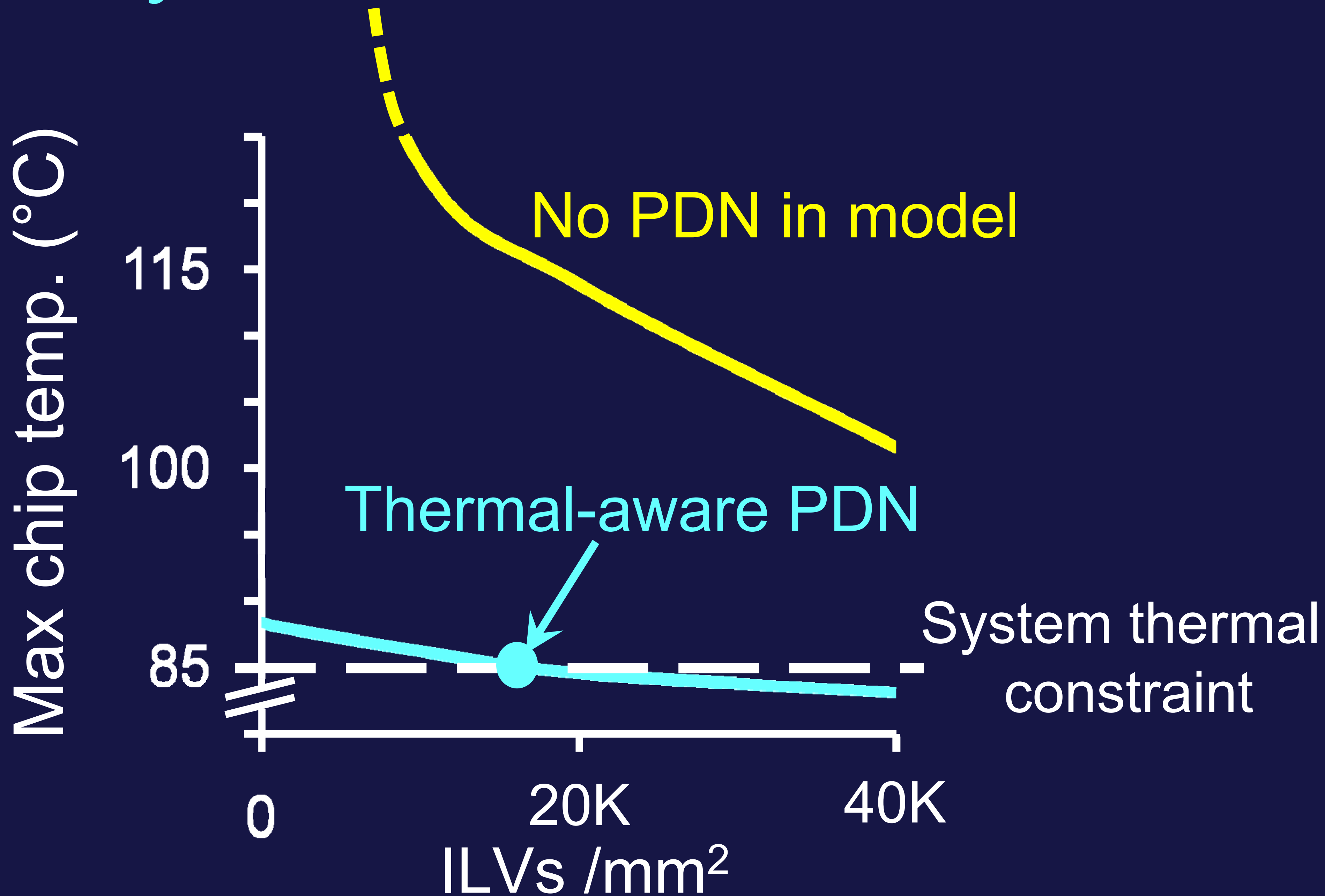
Key Result for Monolithic 3D



Acknowledgement

- FCRP C2S2, NSF
- Prof. H.-S. P. Wong, M. Shavezipur (Stanford)
- Robust Systems Group (Stanford)
- Z. Or-Bach (MonolithIC 3D Inc.)
- TM Mak (Intel)

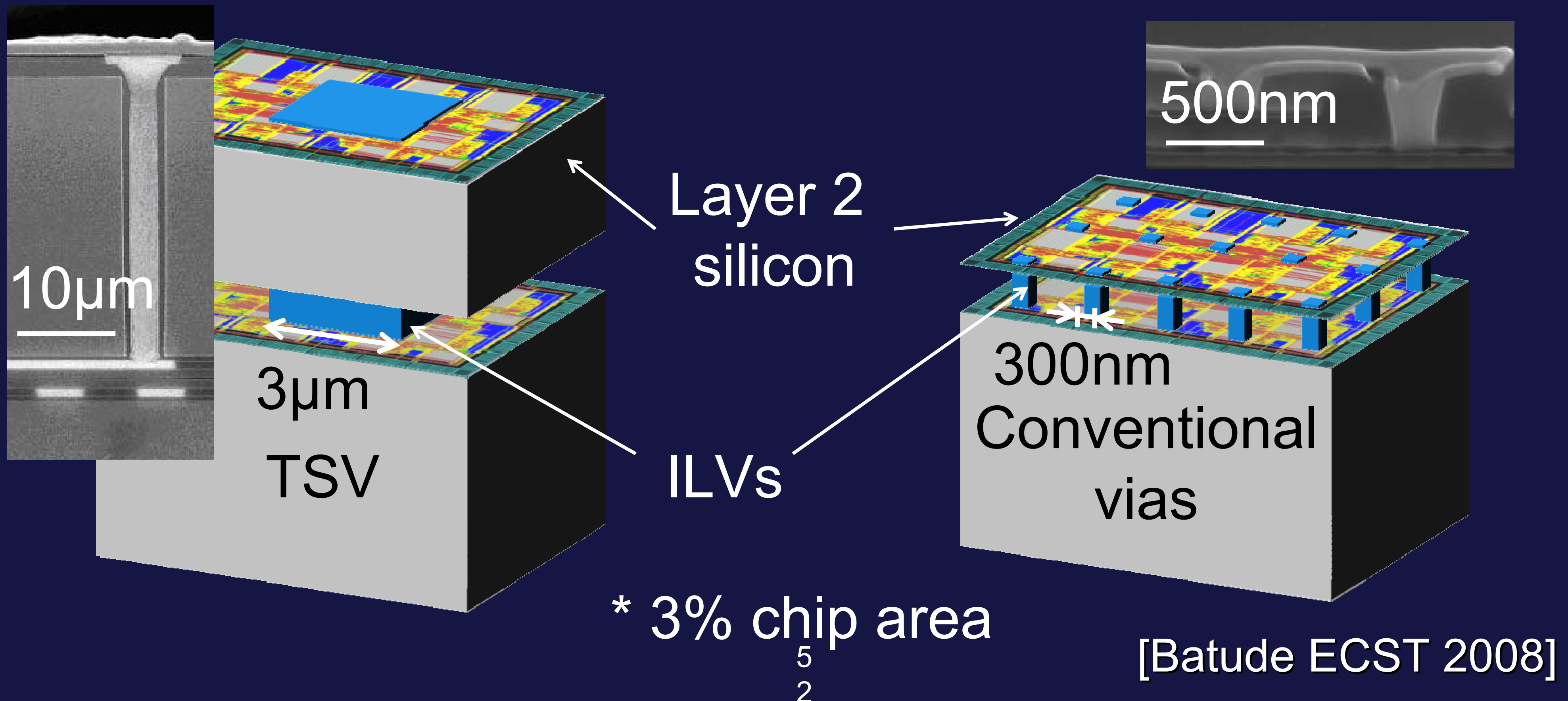
Key Result for Monolithic 3D



Backup slides

Parallel vs. Monolithic 3D

	Parallel 3D	Monolithic 3D
Layer 2 silicon	Thick (> 1µm)	Thin (100 nm)
ILV density*	Low (400/mm^2)	High (40K/mm^2)



* 3% chip area

[Batude ECST 2008]

Existing Tools

	PDNs	Wide range of 3D ICs
Hotspot [Huang TVLSI 06]	✗	✓
3D-ICE [Sridhar ICCAD 10]	✗	✓
This work	✓	✓