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Fusion Bonding for Next-Generation 3D-ICs P. 14

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EVG's integrated fusion bonding platform is designed for 3D/TSV high-volume manufacturing requirements.

COVER

FEATURES

COLUMNS

DEPARTMENTS

Fusion bonding for next-generation 3D-ICs

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Recent developments in wafer bonding technology have demonstrated the ability to achieve improved bond alignment accuracy.

Scaling and Moore's law have been the economic drivers in the planar silicon arena for the last 30 years. During that period, major technology evolutions have been implemented in CMOS processing. The most recent of these evolutions have been extremely complex, including multiple-step lithographic patterning, new strain enhancing materials and metal oxide gate dielectrics. Despite these great feats of engineering and material science, the often predicted "red brick wall" is once again fast approaching and requires evasive action. In fact, several semiconductor suppliers have already shown that the "economic" brick wall has arrived at the 22nm node, where scaling can no longer decrease the cost per transistor [1]. Solutions are getting more difficult to track down in an industry driven by increasing performance at lower cost. 3D-IC integration provides a path to continue to meet the performance/cost demands of next-generation devices while avoiding the need for further lithographic scaling, which requires both increasingly complex and costly lithography equipment as well as more patterning steps. 3D-IC integration, on the other hand, allows the industry to increase chip performance while remaining at more relaxed gate lengths with less process complexity—without necessarily adding cost [1].

While the initial outlook on 3D-IC integration was initially misty, several paths to integration have since been identified, giving an unobscured view to the future in the third dimension [2]. The current state of 3D-IC integration is analogous to crossing the Alps. There are different options to get over the mountain range: by smart use of the valleys, more dangerous direct ascent and descent, or by the brute force of tunneling through. In the end, the most economic routes are combinations of all these factors. In 3D-ICs we see a similar process occurring now. Some 3D devices are established in the middle of the fabrication process, referred as mid-end-of-line (MEOL), while some are established using chip stacking at the back-end-of-line (BEOL). In the future, some 3D stacking will be pulled upstream into the front-end-of-line (FEOL). Which integration scheme will be adopted by a manufacturer depends mainly on the target device, market size and compatibility of processes. The most cost-effective approach to 3D-IC integration should be a combination of all three integration schemes. That said, for many applications 3D-IC integration in FEOL processing offers further potential to pave the way for cost reduction, performance increase and higher-power efficiency.

Front-end processing is still seen as a purely planar-based process, where the power/performance of the device comes from the silicon. However, many disruptive processes and materials, such as SiGe

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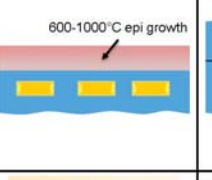
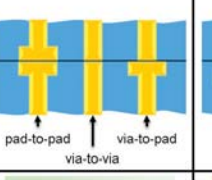
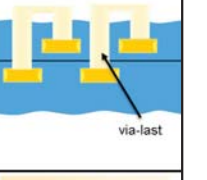
	Epitaxial Growth	Hybrid Bonding	Via-last Integration
			
Integration Density	Medium	High	Medium
Process Temperature	600-1000°C	200-400°C	200-300°C
Process Readiness	Not ready	Yes	Yes
Die Yield	Low	High	High
Complexity	High	Medium	Medium

FIGURE 1. Comparison of different 3D front-end-of-line integration schemes.

and other epitaxial layers, have already been implemented to enable device improvements. As a result, the boundary between planar and 3D stacking has already softened and paves the way for heterogeneous integration (e.g., memory on memory, memory on logic, etc.) to become prevalent going forward [3].

FIGURE 1 provides an overview of different 3D integration process schemes at FEOL. The first integration scheme being considered is layer-by-layer epitaxial growth, which has been a standard process for the semiconductor industry for the last 20 years. However, current epitaxy temperatures, which are in excess of 600-1000°C, make epi not a viable option for 3D integration today, since metal diffusion and broadening dopant distribution of the functional substrate wafer caused by these extreme temperatures would destroy the underlying IC layer. A second integration method is hybrid bonding, whereby a dual damascene copper and silicon oxide hybrid interface serves as both the full-area bonding mechanism and the electrical connection. A third route for 3D integration is the transfer of a thin processed semiconductor layer (ranging from tens to a few hundred nanometers in thickness) using a full-area dielectric bond. In contrast to hybrid bonding, the electrical connection is introduced by a via-last process between early interconnect metal levels on the bottom wafer and the second transferred transistor layer.

Both hybrid bonding and full-area dielectric bonding can be achieved through aligned wafer-to-wafer fusion bonding. However, high-interconnect density along with small routing dimensions set a high bar for bond alignment precision, which is necessary for fusion bonding. Fusion bonding is a two-step process consisting of 1) room-temperature pre-bonding and 2) a high-temperature annealing step. This essentially relates to the chemical bonds at interface. While pre-bonding is based on hydrogen bridges, thermal annealing facilitates the formation of covalent bonds.

An important benefit of fusion bonding is the widespread availability of bonding materials. Any exotic or novel material suffers a high barrier to adoption in the semiconductor industry, in part because it must comply with many different specifications and requires lengthy and extensive failure analysis to ensure no negative impacts are introduced across the entire chip process. With fusion bonding, however, all integration schemes rely on silicon oxide, silicon nitride or oxy-nitrides as dielectric bonding materials, and copper or other interconnect metals—all of which are standard in state-of-the-art IC production lines.

Early on, successful fusion bonding required that the bonding material be transformed into a viscous flow, which required extremely high temperatures (ranging from 800°C to 1100°C depending on doping as well as deposition method) [4]. However, major research has been and continues to be invested in interface physics and morphology prior to bonding and their effect on the bonding result. Recent efforts in low-temperature plasma activation bonding have enabled a reduction of the thermal annealing temperature to about 200°C and opened up the possibility for further material combinations [5,6]. In fact, fusion bonding is already being implemented in high-volume production for certain applications, including image sensors and engineered substrates, such as silicon-on-insulator (SOI) wafers. In the case of wafer-to-wafer fusion bonding, the process can readily being introduced into the CMOS process flow, which uses low-k dielectrics and standard metals.

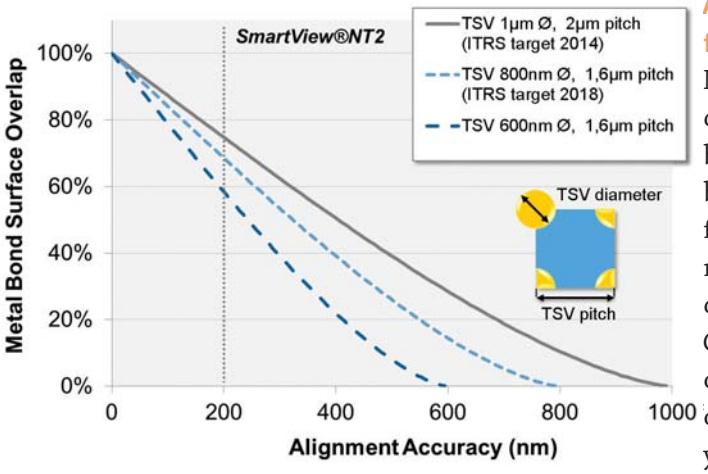


FIGURE 2. Calculated surface overlap of metal TSVs for hybrid bonding as a function of wafer-to-wafer alignment accuracy. Comparison of ITRS roadmap relevant TSV pitches and diameters reveal, alignment accuracy of better than 200nm (3σ) is needed to achieve 60% and more TSV overlap for hybrid bonding.

Alignment is key for fusion-bonded 3D-ICs

Minimizing the via dimension for via-last bonding, or the via and bonding pad dimensions for hybrid bonding, are key requirements for bringing down the cost of 3D devices. Considering that the role of a TSV is essentially only" for signal connection yet consumes valuable wafer real estate, further miniaturization has to be the logical consequence. Increasing integration density is a means of regaining valuable active device area. However, a direct consequence of smaller interconnect structures is the need for improved wafer-to-wafer alignment.

As indicated in the cross section of **FIGURE 1** for via-last processing after semiconductor layer stacking, lithographic etch masks for the vias need to be aligned to the buried metal layers. Bonding alignment is also key here, since the resist layer must match with contacts on both the bottom and top device layers. In order to minimize loss of silicon real-estate and maintain small wiring exclusion zones, the bond alignment must be within tight specifications and adapt to metal, via and contact nodes, as shown in **FIGURE 2**.

The semiconductor world would be easy if devices

operated at a constant voltage. However, a major concern with 3D-IC/through-silicon via (TSV) integration is the potential introduction of high-frequency response and parasitic effects. Again, bond alignment is of major importance here. Any via within the interconnection network will generate a certain electric field around it. Perfect alignment between individual interconnect layers results in a symmetric electric field, whereas misalignment can cause a local enhancement of the electric field. This in turn can result in an electric field imbalance. Further scaling of interconnects and pitch reduction between vias means that inhomogeneous electric fields gain importance. Memory stacking and high-bandwidth interfaces with massively parallelized signal buses are particularly sensitive to this issue [2].

bonding [7]. The newly introduced SmartView®NT2 bond aligner has demonstrated the ability to achieve face-to-face alignment within 200nm (3σ), as shown in **FIGURE 3**.

Several factors contribute to the global alignment of the wafers besides the in-plane measurement and placement of the wafers relative to each other. In fusion bonding, both wafers are aligned and a pre-bond is initiated. When bringing the device wafers together, wafer stress and/or bow can

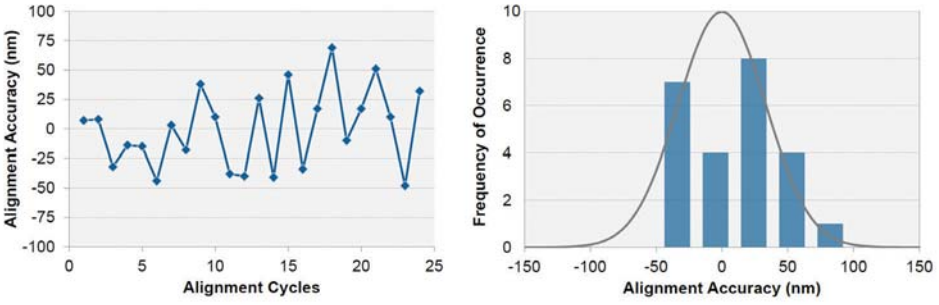


FIGURE 3. SmartView®NT2 alignment data for consecutive alignments (left), revealing an alignment accuracy of 200nm (3σ) from the histogram and corresponding normal distribution (right).

Optimizing alignment values

From the above discussion, it becomes clear that wafer-to-wafer alignment accuracy for fusion bonding has to be in line with interconnect scaling. The 2011 edition of the International Technology Roadmap for Semiconductors (ITRS) roadmap (at the time of writing this article, the Assembly and Packaging section of the 2013 ITRS Roadmap has not yet been published) specified that for high-density TSV applications, the diameter of vias will be in the range of 0.8-1.5 µm in 2015 [2], which requires an alignment accuracy of 500nm (3σ) in order to establish a good electrical connection. Previous studies have demonstrated that alternative wafer-to-wafer alignment approaches can achieve a post-bond alignment accuracy of better than 250nm for oxide-oxide fusion

influence the formation of a bond wave. The bond wave describes the front where hydrogen bridge bonds are formed to pre-bond the wafers. Controlling the continuous wave formation and controlling influencing parameters is key to achieving the tight alignment specifications noted above. In essence, optimizing a fusion bonding process means that one must optimize the force generated during the bonding.

For example, bowing and warping of processed wafers can be substantial after via etching and filling. TSVs in particular represent local strain centers on a wafer. Minimizing the via size and depth helps to reduce the strain, which heavily influences the shape and travel of the bond wave. At the same time, this bond wave also causes local strain while running through the bonding interface. Any wafer strain manifests in distortion of the wafer, which leads to an additional alignment shift. Process and tool optimization can minimize strain and significantly reduce local stress patterns. Typically, distortion values in production are well below 50nm. Indeed, further optimization of distortion values is a combination of many factors, including not only the bonding process and equipment, but also previous manufacturing steps and the pattern design. To a large extent, plasma activation also determines initial bonding energies, which impact the travel and formation dynamics of the bond wave and consequently wafer distortion.

Conclusion

In summary, aligned fusion wafer bonding is progressing rapidly to support front-end 3D-IC stacking. However, wafer bonding alignment accuracy must improve in order to meet the production requirements for both current and future design nodes. Controlling the local alignment of the wafers is only one aspect. Other important aspects include the initiation, manipulation and control of the bond wave. Recent developments in wafer bonding technology have demonstrated the ability to achieve bond alignment accuracy of 200nm (3σ) or less, which is needed to support the production of the next generation of 3D-ICs.

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