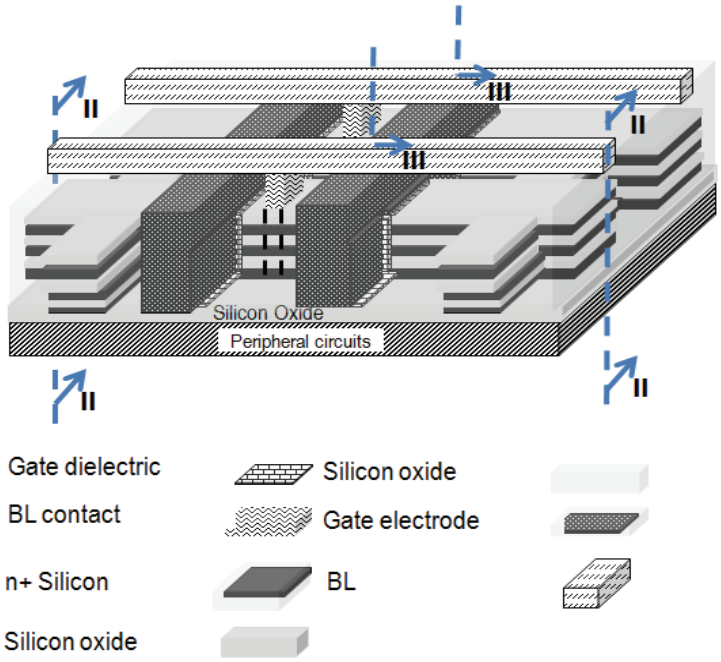
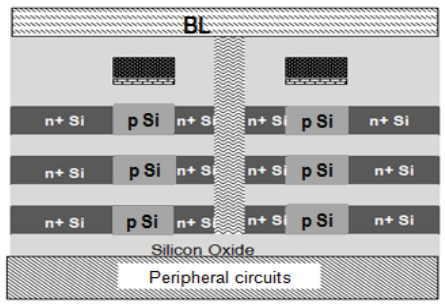
MonolithIC3D™

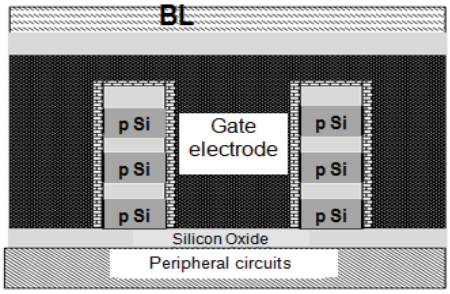
Technology Breakthrough

Monolithic 3D DRAM





View along II plane



View along III plane

Technology:

The monolithic 3D IC technology is applied to producing a monolithically stacked single crystal silicon double-gated floating body DRAM memory. Peripheral circuits below the monolithic memory stack provide control functions.

Monolithic 3D IC provides a path to reduce DRAM bit cost without investing in expensive scaling down.

See reverse side for more on details monolithic 3D IC technology & DRAM flow

Benefits:

- 3.3X the density of conventional stacked capacitor DRAM
- Same number of litho steps as conventional stacked cap DRAM
- Single crystal silicon on all layers
- Scalable: Multiple generations of cost-per-bit improvement for same equipment cost and process node: use the same fab for 3 generations
- Forestalls next gen litho-tool risk
- Avoids the red bricks and costs of capacitor scaling& new cell transistor development

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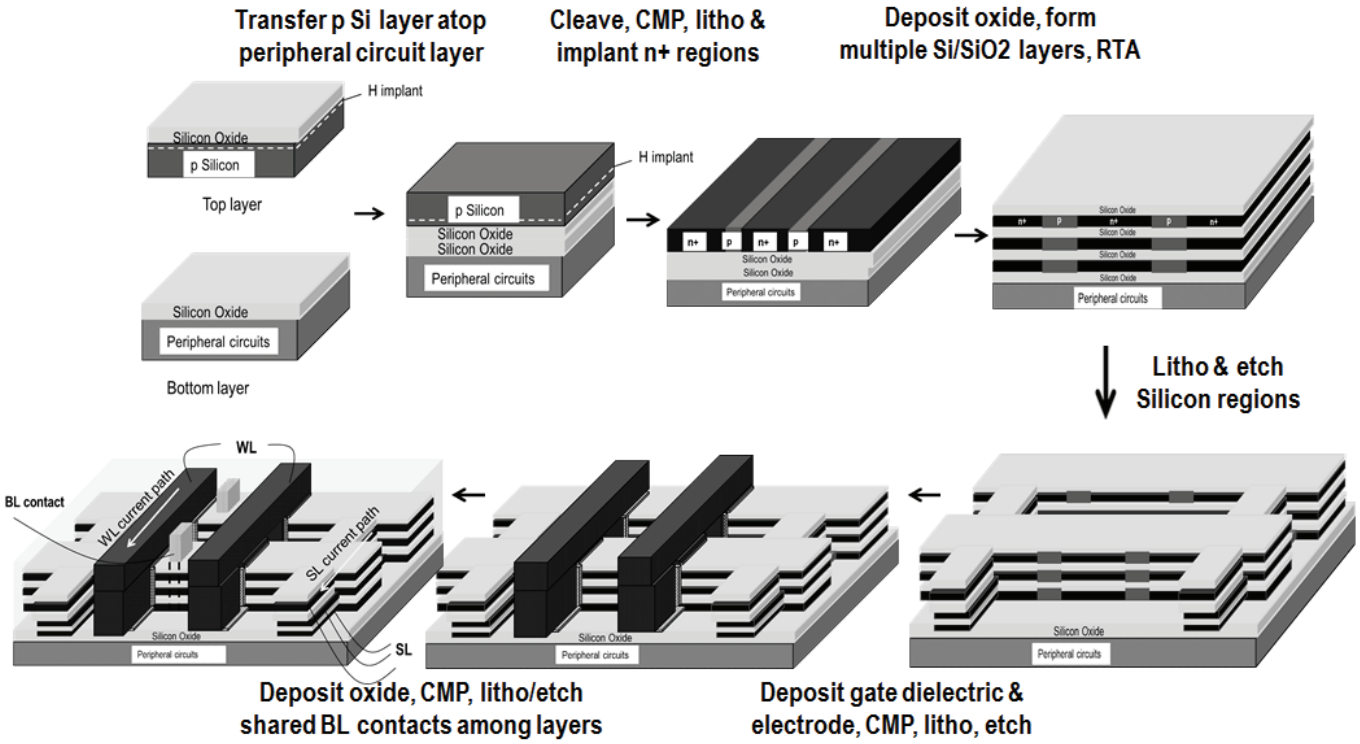
www.monolithic3d.com. ◆Patents pending

Technology Breakthrough

Our 3D DRAM technology innovatively combines these well-studied technologies:

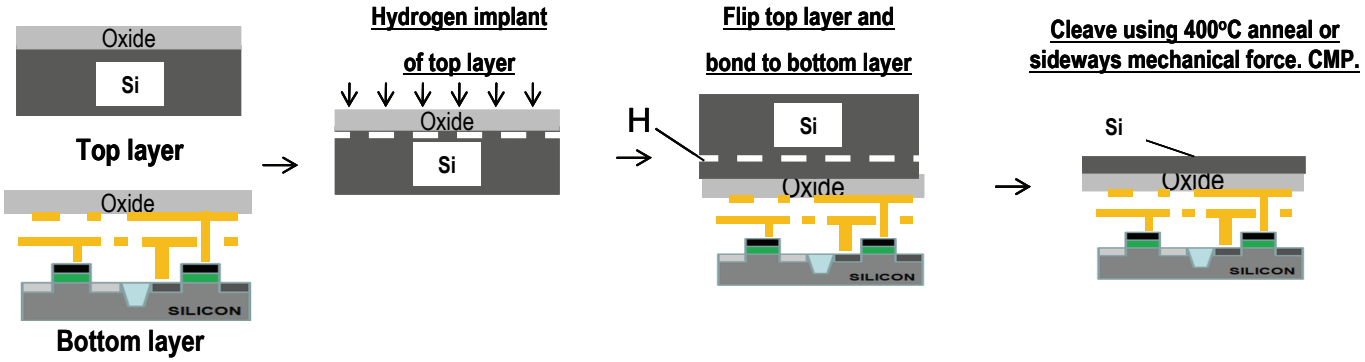
- Monolithic 3D with litho steps shared among multiple memory layers
- Stacked Single crystal Si with ion-cut
- Double gate floating body RAM cell with charge stored in body



Layer Transfer Technology ("Ion-Cut")Defect-free single crystal obtained @ <400°C

Leveraging a mature technology (wafer bonding and ion-cleaving) that has been the dominant SOI wafer production method for over two decades.

Innovate and create multiple thin (10s – 100s nanometer scale) layers of virtually defect free Silicon by utilizing low temperature (<400°C) bond and cleave techniques, and place on top of active transistor circuitry. Benefit from a rich layer-to-layer interconnection density.



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