Chip Scale Review

January - February 2013 Volume 17, Number 1

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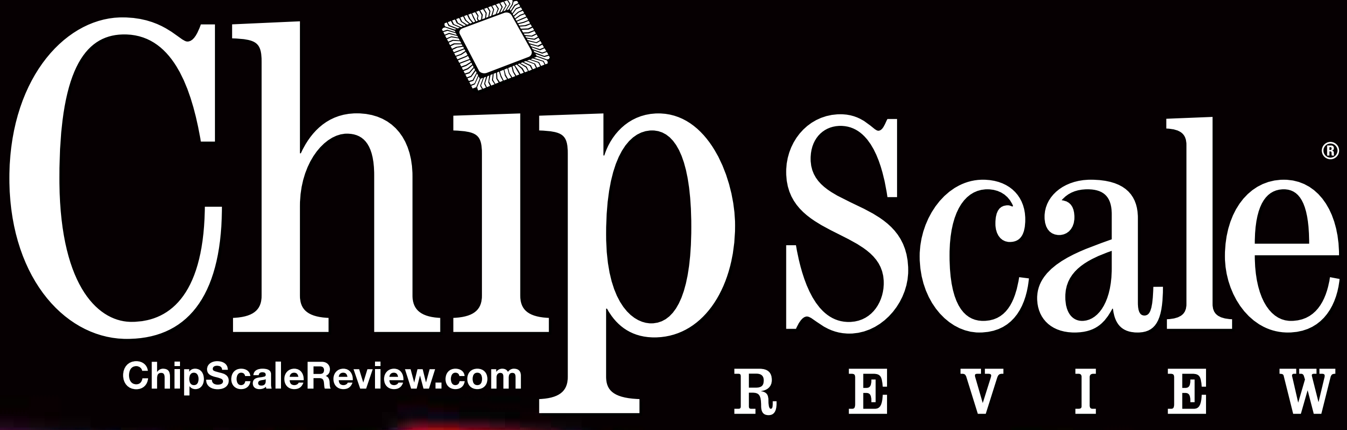

The International Magazine for the Semiconductor Packaging Industry

Volume 17, Number 1

January - February 2013

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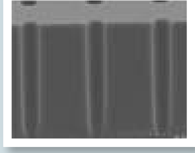
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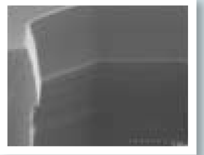
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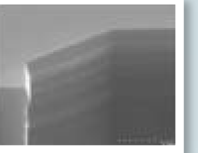
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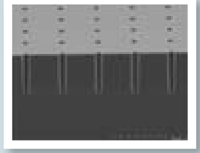
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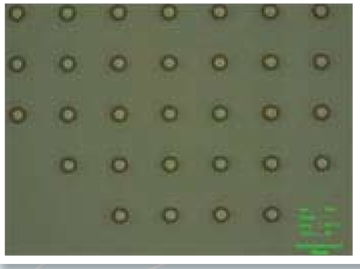
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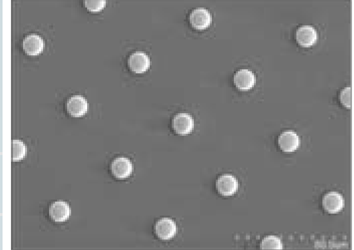
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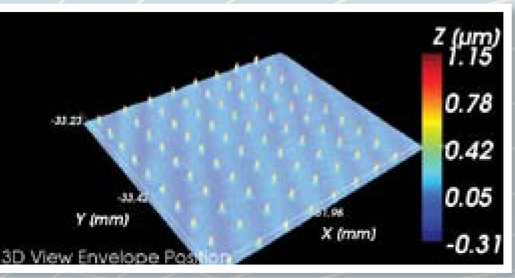

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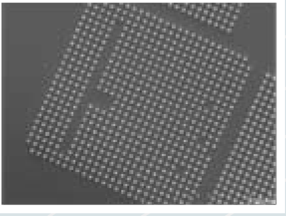

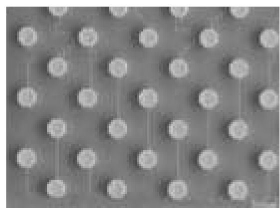

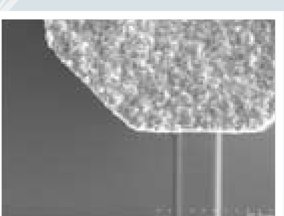

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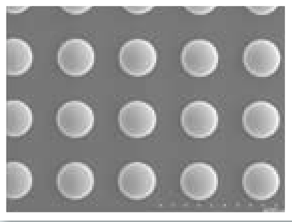

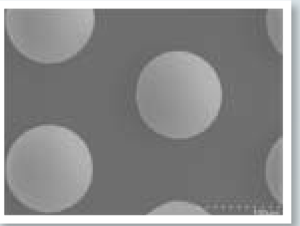

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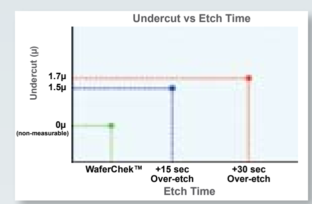

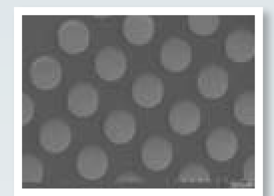
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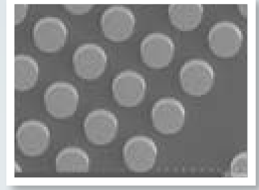
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The International Magazine for Device and Wafer-level Test, Assembly, and Packaging Addressing High-density Interconnection of Microelectronic IC's including 3D packages, MEMS, MOEMS, RF/Wireless, Optoelectronic and Other Wafer-fabricated Devices for the 21st Century.

The cover photo shows Bond Via Array™ (BVA™) PoP technology from Invensas. It enables 1000+ memory-logic IO utilizing free-standing wire structures in lieu of TSVs. The technology addresses the industry's need for increasing the performance of processor-memory interconnect as it transitions from single core to multi-core CPUs, while also handling the requirements of low-power computing and cloud computing. It can be used in applications such as 3D packaging, embedded packaging, and WLP.

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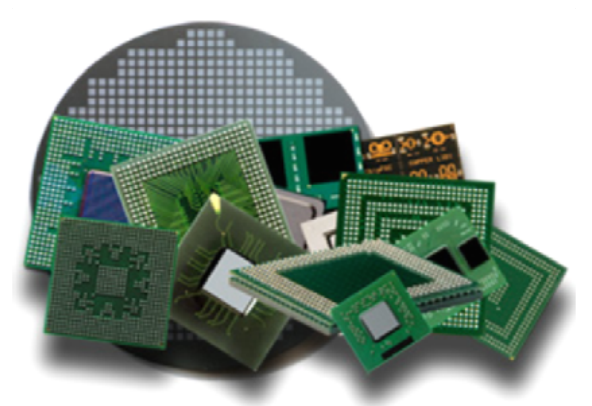

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FROM THE PUBLISHER

Of the Industry, By the Industry, & For the Industry

Happy New Year to all! As we closed out 2012 with a U.S. presidential election and having avoided sailing over the fiscal cliff and yet surviving the end of times per the Mayan Calendar, we speculate what the New Year has in store. What I see and hear from economic forecasters and industry experts reflect the standard debate between the optimistic and pessimistic perspectives that were consistent with the prognostications of last year and indeed every year!

All industrial sectors will be looking to take advantage of interest rates by making capital investments in new equipment and facilities, as well as looking for strategic acquisitions and joint development opportunities and initiatives including 22nm and 450mm technologies. These were evidenced recently by Intel, Samsung and Taiwan Semiconductor's significant equity investments that range in the billions of Euros (€) with ASML for development of next-generation lithography systems and technologies that will be suitable for patterning 450 mm silicon wafers. The downstream effect will result with supply chains requiring adaptations to accommodate demands. Companies will increasingly make investments in additional technical staff, support and senior management hires.

At the start of the New Year, CSR announced a new Chair of the magazine's Editorial Advisory Board, Dr. Andy C. Mackie, Senior Product Manager at Indium Corporation. Andy sees 2013 as the year when large-scale implementation of 2.5D into the two main driving applications (mobile devices and lower-power servers) will occur with 3D (memory plus logic) finally also emerging in a prototype form. His company, like many, continues expansion into the Asia-Pacific markets with semiconductor and advanced assembly materials, especially in fluxes and similar materials for flip-chip and 2.5D/3D manufacturing and assembly and several offerings into the high-temperature lead-free power semiconductor market space.

With a new editorial board of advisors and a commitment to editorial excellence, I asked the staff at CSR "What does it take to continue CSR's excellence?" The unequivocal answer remains, tons of PhDs, scientists, engineers and technologists from many disciplines that contribute insightful research articles and the continuing support of our subscribers and advertisers. I completely agree!

This edition of CSR is packed with terrific articles by our industry's top authors. We cover BVA PoP, MEMS process solutions, Plasma FIB circuit modifications, cost efficient WLP stacking, WLP functional testing and HVM of 3D, IC packaging economic trends and the obvious requirements of burn-in & test sockets. It is a cover to cover read.

CSR is firmly in the positive-outlook camp for 2013. Jeanne Beacham of Delphon Industries concludes with a great outlook as well: "I am a true optimist and believe that despite today's economic uncertainty, there are plenty of opportunities for growth."

So as an industry, let's spend 2013 investing in the future. We're still here and you, our readers deserve nothing less than the best of the industry, by the industry and for the industry.

Kim Newman
Publisher

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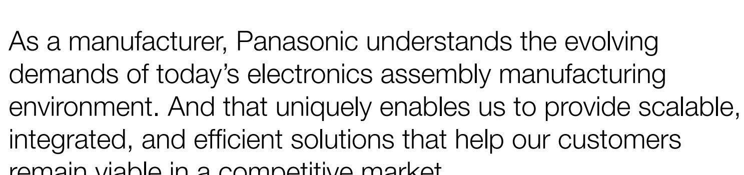

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Global Economy Drives the IC Industry's Cycle

By Bill McClean [IC Insights, Inc.]

Throughout 2012, the expectations for global economic growth consistently deteriorated. Global GDP is estimated to have expanded by only 2.6% in 2012. It should be noted that 2.5% or less worldwide GDP growth is typically considered a global recession (annualized 3Q12 worldwide GDP growth was only 2.5%, equal to the global recession threshold figure). Moreover, IC Insights' forecast for 2013 worldwide GDP growth is 3.2%. Although this figure is higher than the 2.6% growth rate of 2012, it would still be 0.3 points below the 3.5% long-term average.

One of the primary reasons for weak 2012 worldwide GDP growth was the negative GDP growth registered by the Eurozone and U.K. economies. Moreover, the Eurozone is not expected to display a strong rebound, with 0.0% GDP growth forecast for the Eurozone economy in 2013.

China's GDP growth is estimated to have dropped to only 7.7% in 2012 with a modest rebound to 8.1% growth forecast for 2013. While many developed countries would welcome 7% or higher GDP growth rates, for China, this figure is significantly below the 10% and greater annual GDP increases logged from 2002-2009. In an attempt to address its economic "slowdown," the Chinese government was quick to inject stimulus into its economy starting in the second half of 2012 by aggressively lowering interest rates as well as enacting $156 billion in construction project programs. While this stimulus was too late to have had a significant positive affect on its 2012 GDP growth, China's GDP is likely to get at least a modest boost from this stimulus activity in 2013.

While the correlation between worldwide GDP growth and IC industry growth has historically been good (not great), IC Insights believes that the correlation in 2013 will be very good, as it was in 2012. Using a worldwide GDP forecast of 3.2%, the most likely range for IC market growth in 2013 is 3-7%.

Including the U.S. presidential election year of 2012, over the past 11 U.S. election years since 1972, worldwide GDP growth averaged 3.9%, while semiconductor industry growth averaged 22%. Moreover, the semiconductor industry grew 10% or better in 8 of the past 11 U.S. election years. The three election years when the semiconductor industry did not grow 10% or better (1996, 2008, and 2012), it registered single-digit declines (with a 1% decline occurring in 2012).

The election-year cycle is one reason why IC Insights has identified 2013 as a possible "slow" year in the worldwide economy and semiconductor industry. Over the past 10 post-U.S.-election years, worldwide GDP growth averaged a below-average 3.1% with worldwide semiconductor industry growth averaging only 4%. Moreover, worldwide semiconductor industry growth exceeded 8% in only three of these 10 post-election years (1973, 1977, and 1993), and only once since the late 1970s.

Oftentimes the "problem" with post-U.S.-election years is that many of the subsidies and stimulus measures enacted during an election year are withdrawn or allowed to expire after the election is over. In the case of the U.S., there is likely to be continuing debate and consternation in Congress over whether to keep the payroll tax cuts (unlikely to be extended) and how much to raise existing tax levels in 2013. Although the exact outcome regarding the future U.S. tax structure and budget is unclear, the large amount of uncertainty created by these issues is expected to be a "headwind" on economic growth in 2013. Because of this, the U.S. economy is forecast to show only a modest rebound in 2013 before picking up momentum in 2014.

As mentioned earlier, the correlation between global economic growth and semiconductor industry growth has been relatively good (see **Figure**). In some cases, when the semiconductor market and worldwide economy are moving in opposite directions, the semiconductor industry is usually encountering an inventory "burn" (e.g., 1985), significant overcapacity (e.g., 1996 and 1997), or significant under-capacity (e.g., 1993).

IC Insights believes that the semiconductor industry cycles are becoming increasingly tied to the health of the worldwide economy. While poor semiconductor industry growth has occurred during periods of strong worldwide economic growth, primarily due to semiconductor industry overcapacity and the resulting IC price declines, it is rare to have strong semiconductor industry growth without at least a "good" worldwide economy to support it. Thus, through the forecast period of 2016, annual global semiconductor market growth rates are expected to closely mirror the performance of worldwide GDP growth.

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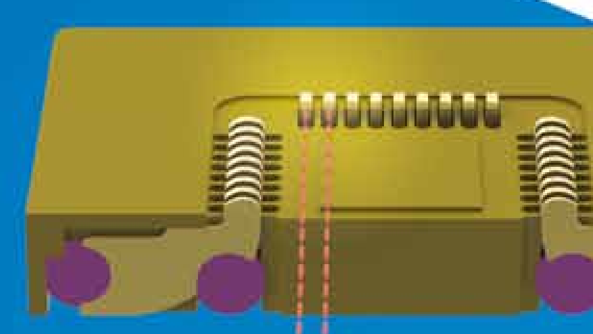

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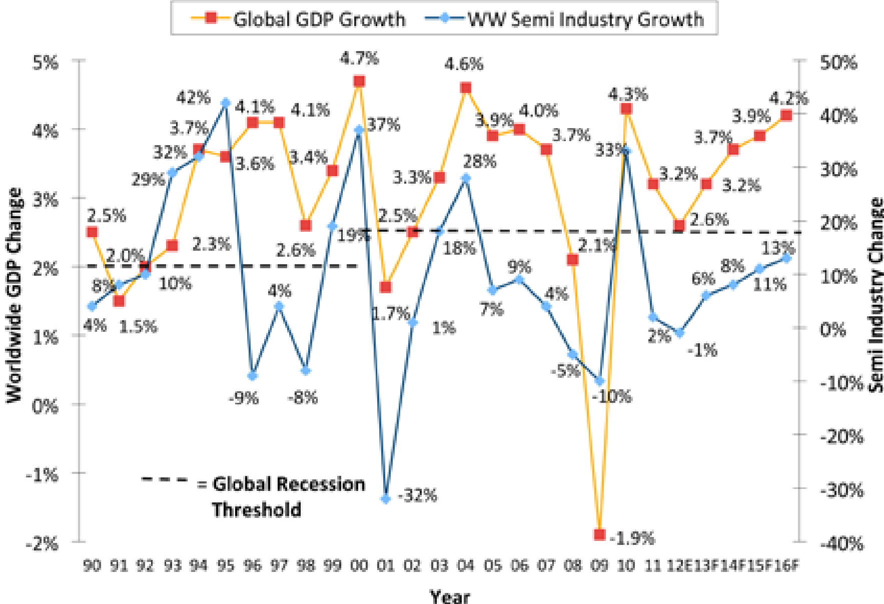

Figure. 1990-2016 Semiconductor Industry Growth vs. Worldwide GDP Growth. SOURCE: IC Insights

IC Packaging Trends

Total IC unit shipments enjoyed seven consecutive years of growth (2002-2008) before they dropped 7% in the recession year of 2009. Units then rebounded with 29% growth in 2010 and another 2% growth in 2011. IC unit shipments were flat in 2012 but are forecast to display average annual growth of 5% from 2011 to 2016.

IC packaging has evolved from the "old" DIPs (dual in-line packages) to a variety of packages ranging from ultra-thin SO (small-outline) packages and CSPs (chip-scale packages) for low-pin-count applications to BGAs (ball grid arrays) and MCPs (multi-chip packages) with thousands of solder ball (or bump) connections.

It is within the newest package categories that the real diversity starts to show. For example, there are BGA designs to meet nearly any packaging need. BGAs can be plastic, tape, or ceramic, wire bonded or flip-chipped, cavity-up or cavity-down, overmolded or encapsulated, single-chip or multi-chip. They can have lead counts ranging from less than 100 to thousands. They may be made very small and thin for portable electronics, or thermally and electrically enhanced for high-speed systems.

The options for mounting multiple chips in a single package solution have become very diverse. Dice can be placed side-by-side in MCM- or BGA-type packages, numerous dice can be stacked on top of each other in packages the same size as single-chip packages, packages can be stacked atop other packages, bare dice can be bonded together to create a 3D integrated circuit. Additionally, some combination of any or all these technologies can be used to meet the space requirements and/or performance needs of each particular system application.

Shown in the **Table** is IC Insights' IC unit shipment forecast by package type, which has been updated to reflect the latest expectations for unit growth over the next several years. Advanced packages such as bare die and wafer-level devices continue to grab market share from older package types, but the mainstay of package types—SO and FP/CC-type packages—were the most widely used in 2012 and are expected to be the most popular throughout the forecast period. Low-lead-count SO packages are used primarily in the packaging of analog and standard logic ICs but can also be found in most other IC categories.

For larger chips, with lead counts that exceed the capability of SOs, LCCs (leaded chip carriers) and QFPs (quad flat packages) are the most widely used package types. Like the SOs, these peripherally leaded packages can be found in just about every IC category. However, the lead counts of LCCs and QFPs are limited to a maximum of about 80 and 400 pins, respectively. BGA-type packages have displaced QFPs, as well as through-hole mounted PGAs, in most applications. BGAs offer the advantages of the extensive use of existing surface-mount technology infrastructure, high board-level assembly yields, superior electrical

IC Package Shipment Trends (Billions of Units)

Package Type	10	11	12E	13F	14F	15F	16F	11-16 CAGR	Examples
SO	65.4	62.0	62.5	64.1	67.0	70.8	76.3	4%	TSOP, SSOP, SOJ, LOC, SOT, SC
FP/CC	44.2	44.8	45.5	48.1	51.0	54.8	59.7	6%	QFP, QFN/MLF, Flatpack, PLCC, LCCC, Cerpack
BGA (incl. MCP)	32.1	34.6	37.3	40.3	43.6	47.3	51.9	8%	PBGA, FPBGA/µBGA, TBGA, LGA, CGA, SiP, S-CSP, MCM-BGA
Bare Die	10.1	11.5	12.9	13.6	15.0	16.7	18.8	10%	FCOB, COB, COG, COF, TCP
Wafer-Level	8.7	9.6	10.5	11.3	12.7	14.7	16.5	11%	Ultra CSP, microSMD, eWLB
MCM	1.1	1.1	1.3	1.3	1.4	1.6	1.8	9%	Multichip Modules
Through-Hole	7.9	7.7	7.7	7.6	7.5	7.6	8.0	1%	PDIP, CERDIP, ZIP/SIP, TO, PGA
Total	169.6	171.3	177.6	186.3	198.4	213.5	232.9	6%	

Note: CSPs are included but not considered a distinct package category.

Table. Package Shipment Trends (Billions of Units). SOURCE: IC Insights

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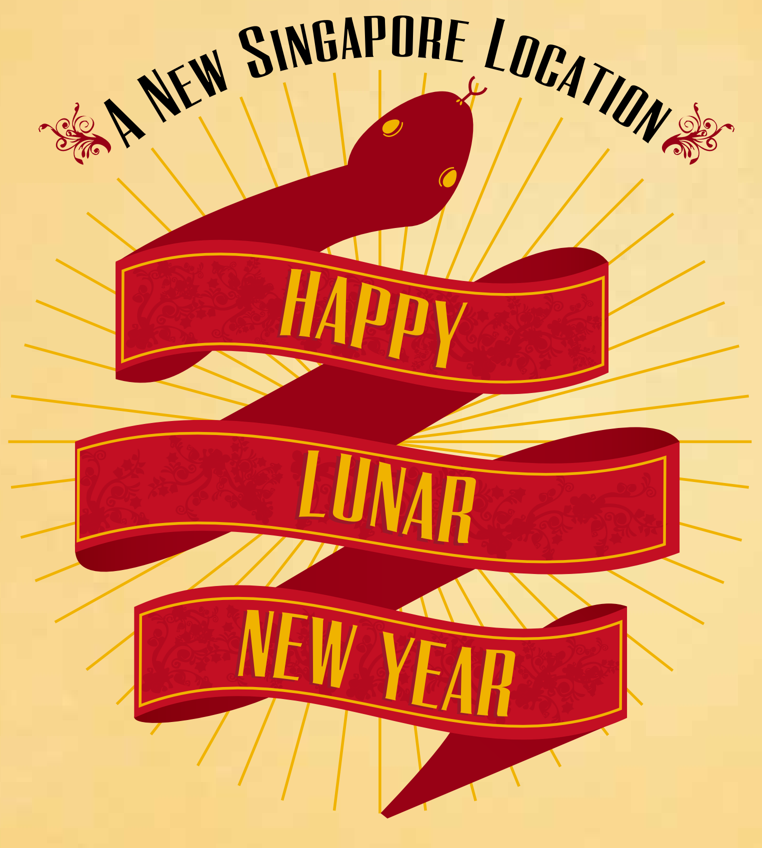

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ABOUT PLASTRONICS

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performance, and higher I/O capability.

Over the next five years, some of the IC packages that will enjoy the strongest growth in demand will be standard and fine-pitch BGAs, multi-chip packages like stacked CSPs, package-on-package assemblies, quad flat no-lead (QFN) packages such as bumped chip carriers or micro-lead frame devices, and wafer-level packages (WLPs). Three-dimensional ICs built using through-silicon via (TSV) technology are all the rage in the news, but 3D ICs will likely remain a niche technology until after 2013 because there are still several challenges to overcome with this relatively new technology including thermal management issues and test access for individual wafer/die.

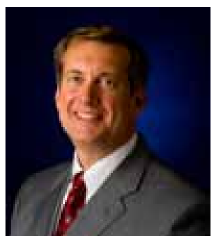
The group of packages that are considered "advanced," including BGAs, CSPs, WLPs, and flip-chip-on-board (FCOB) solutions, represented about 40% of total IC package shipments in 2012. That share is expected to grow to 43% by 2016.

Overall, there are a multitude of IC packages currently in use or under development. The wide variety of packages is driven by the fact that system manufacturers increasingly want personalized packages at commodity prices. These are packages with an optimal balance of thermal and electrical performance, real estate constraint, and low cost, mixed and matched to meet the needs of each particular system application—all in standard outlines or at least built with standard processes.

The integrated circuit industry will continue to enable more powerful machines at lower prices and the packaging industry will play an increasingly important role in making it happen. Developments in wafer-level packaging, system-in-package, and the imminent 3D revolution will enable scaling advances in packaging through 2016. To date, the packaging industry has done a good job of overcoming technology hurdles, but more challenges are in store. Fortunately, global cooperation has so far been good and roadmaps are fairly well-aligned that help address demands for new package architectures, new materials, new processes, and new equipment. All of these will be needed as IC manufacturers begin to move their manufacturing processes to 14nm and smaller line widths.

Biography

Bill McClean received his BS in business administration and an Associate Degree in aviation from the U. of Illinois; he is President of IC Insights, Inc.; email info@icinsights.com



Requirements: Aren't They Obvious?

By David Barnum [Sensata Technologies]

Our business is very exciting because we actually turn raw materials into finished goods that are validating building blocks to other higher level electronic systems that improve and touch our lives in so many ways, every day. The business of designing a burn-in socket, constructing it, delivering it on time, and at a value that meets the customer's expectation, is in itself, a significant accomplishment requiring a lot of information, with no one application exactly the same as another.

Burn-in sockets are subject to thermal and electrical stress, in a controlled environment, for the purposes of inducing the failure of "marginal" semiconductor devices, or those that have inherent defects resulting from manufacturing excursions that cause time- and stress-dependent failures. Translation: burn-in sockets try to induce a failure to prevent marginal semiconductor devices from getting into mission critical, or high-value systems.

Burn-in sockets have a number of sensitivities associated with them. Because we are trying to force failures, they are presented with many types of temperature, humidity and duration profiles, and many types of manual, automatic, and semi-automatic operations are used to present the chip to the burn-in sockets, which are usually mounted on a multi-site burn-in board. In addition, there are many types of chambers and stacking geometries that come into play to process all of the devices needed to be burned-in, in a timely manner.

If we start to list the number of considerations, given the dimensions of the challenge, the list of items is comprehensive, but crucial in attaining the goal of getting the right product for the right customer application. As engineers, we usually leverage our background and make many assumptions that sometimes lead to a win, but sometimes miss the mark considerably. To better approach the challenge, a list of requirements along with the particular package drawings are keys to presenting a winning solution. Listed below are descriptions of some of the more critical requirements and key factors enabling winning burn-in socket designs.

1. **Mechanical outline of the package (including final thickness) with the pad or ball dimensions, and the package's material composition**. As long as the package mechanicals stay stable throughout the development there are usually minimal issues here. If the package thickness or material composition changes between initial definition and final state, then real issues will occur to the point where the socket will not work initially.

2. **Burn-in equipment's or burn-in test condition's electrical requirements: resistance, capacitance, inductance, power requirements**. Usually, these are well defined, but sometimes there are discrepancies in power per pin requirements, which again challenge the socket's ability to perform in the burn-in protocol.

3. **Burn-in test condition's cycling dwell times and profile: how long and at what intervals do the parts see heat, cold and get tested electrically**. This issue has come-up many times as users try to induce failure in their devices. Thermal creep and set of both plastic and contacts can occur, dependent on dwell times at elevated temperatures for both the device and the socket, which can lead to catastrophic failures.

4. **Applied loading and unloading/ packaging equipment mechanicals**. This is sometimes a huge issue in high pin count devices (>350 contacts) and in production environments where handling can shorten socket life substantially. The termination load of the socket cover can limit the amount of sockets used per board or loading fixture, or an individual operator's ability to load the socket. The physical handling of the board from loading fixture to oven and back to packaging has a substantial effect on the sockets near the edges of the burn-in board, as many times we see broken parts from handling issues.

5. **Height of contacts off board, the termination datum, board-to-board spacing, and socket density on the burn-in board**. In a production environment, these are requirements, as they determine how much mechanical stress the sockets and corresponding equipment will see, which will determine how long both sides of the system will endure.

6. **Operating temperature requirements**. These requirements include those for the device under test, and those mechanical (board-to-board or rack spacing) and electrical constraints of the system (power availability beyond the basic controller), relative to the use (or not) of a passive heat sink, active heat sink, chamber

control, or local control. Some socket companies can add value in the design of the complete system, which, if defined in the beginning, can lead to a very robust and flexible system for future requirements.

7. **Cycling: a practical amount of durability cycles are needed**. Users want the maximum available for "design security;" however, many times the requirements are well above the life of the particular device being burned-in.

Most of the time the first and second items listed above are provided, which gets us to first base. However, what is critical in the success of the program is an understanding of the remaining items in the overall execution of a robust and value-oriented design. Socket OEMs certainly understand that many times users want to "stack" the requirements and use certain "production" level sockets, which have been optimized for one set of conditions with many other conditions for which they were not intended. Unfortunately, this usually ends-up with a call into the OEM describing failures. Other times, the design of a new socket misses the mark because Items 3-7 were not fully comprehended, or communicated upfront, which is usually a shared responsibility between parties. Item 7 is always an interesting subject to discuss, as cost via contact design is a huge determining parameter regarding the practical amount of cycles required. The real key is how the parts are used in a production environment.

In summary, requirements for robust and value oriented burn-in socket designs are dependent on a whole host of requirements that are sometimes not given enough time to be thoroughly understood, as many times the socket OEMs are brought in towards the end of the chip development cycle. As can be seen from the list above, there are many things to comprehend when designing a burn-in socket. While for the most part, the industry does a good job on both sides of the equation, we do experience enough "hiccups" to inspire the holistic set of requirements such as those presented above to ensure successful execution in any burn-in application. In this business, there are a plethora of packages that can house die. It is incumbent on all of us to work together to better define requirements upfront to produce better outcomes for both the supplier and the user of burn-in sockets.

Biography

David Barnum received his BS degree in mechanical engineering from the U. of Massachusetts-Lowell, and studied finance, operations management and marketing at the U. of New Haven. He is senior director and global business unit manager at Sensata Technologies; email dbarnum@sensata.com

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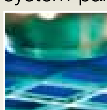

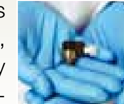

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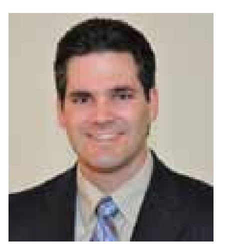

Robust Process Solutions for MEMS Flip-Chip Applications With Medium Density Lead-Free Solder Interconnects

By Dave DiPaola [DiPaola Consulting]

With the proliferation of MEMS in sensor products in a variety of applications, packaging challenges continue to be at the forefront of successful production launches. Furthermore, package shrinkage, cost pressure and rapid time to market magnify these challenges because traditional approaches can no longer meet these constraints. The four major packaging challenges that consistently appear in product development are electrical interconnection, mitigating the effect of packaging strains on sense element performance, protecting the sensor from the environment, and proper management of temperature distribution and resulting material behavior. Given the complexity of these topics, this article will review the challenges in electrical interconnection for increasingly smaller MEMS flip-chip applications using lead-free solder for medium density I/O, size sensitive medical applications. With bump sizes of 90µm and bump pitch of 150µm, particular attention in component handling, material selection and process development were required to overcome challenges of poor reflow due to oxidation and shorting, while minimizing tooling and process cost. In particular, cleanliness, material handling, flux selection and application, metallization and reflow profile tuning are reviewed in detail for a robust design.

Challenges of Lead-free Solder Interconnects

There are several factors that increase the difficulty of lead-free solder interconnects with medium density I/O for MEMS flip-chip applications. These factors include high reflow temperature, increased surface area of the bump relative to its volume, flux and cleaning limitations, necessity for underfill and tight I/O spacing. In the transition from Sn-Pb solder to those containing solely tin, tin, copper and silver, or other variants, the metal or alloy melting temperature increased requiring higher reflow temperatures to ensure proper wetting of the joint. This higher temperature causes oxidation to develop more quickly on metallization and solder making it more difficult to obtain a properly wetted bump. This problem becomes even more challenging as bump size decreases and the bump's external surface where oxide is present becomes a larger percent of the total solder volume. Therefore, the ratio of oxidized to non-oxidized solder increases and increased heat is needed to overcome this effect creating an undesirable cycle that cannot be sustained. Flux is used to prevent oxide growth and remove it from the bumps' external surface during reflow. However, aggressive fluxes cannot be used because of their corrosive nature, ionic contamination and inability to be cleaned post reflow. The fragile nature of MEMS devices for medical applications and the narrow gap between chip and substrate make cleaning post reflow ineffective or not practical due to product damage. Underfill is also a requirement in this application to prevent shorts from tin whiskers between bumps and to minimize stress on the bumps from temperature fluctuations for medical products located outside of the body. The tight I/O spacing also results in a smaller process window to prevent solder shorting. Despite these challenges, there are a number of combined steps that can be taken to create robust lead-free interconnects.

Process Considerations

Product cleanliness and material handling are crucial but often overlooked steps in creating a robust solder joint. Rigid and flexible printed circuit boards readily absorb moisture and this moisture is outgassed from the product during reflow thereby increasing oxide growth on the bump. To prevent this, circuit boards can be pre-baked at 125°C for 2-6 hours (depending on environmental exposure and moisture present) in an oven to drive off moisture prior to reflow. In addition, metallization on the substrates should be selected to minimize oxidation growth during this step. If the substrate is bumped rather than the MEMS flip-chip, another option is to ship the products in vacuum sealed, desiccant bags and store them in nitrogen back-filled

chambers when not being processed to limit exposure to humidity and oxygen. Product cleanliness is equally important because specific contaminations such as sodium chloride can accelerate oxidation growth and ionic contamination can create shorts in the presence of moisture. Clean process environments and aqueous-based cleaners followed by post bake are often effective.

The cleaning action of flux to remove oxide is another critical step to a proper solder reflow process. Without the post reflow cleaning option for many medical MEMS devices, rosin-based ROL0 fluxes without halides that completely evaporate during reflow are recommended for use. The use of halides in fluxes provide better cleaning action but are avoided because of their corrosive nature and they cause ionic contamination that can lead to shorts without cleaning. One flux option that provides more aggressive cleaning but contains no halides is ROM0. It is best to limit flux application to the lower half of the bump covering 30-50% of its surface. In some cases, more flux is required to clean the oxide present and maintain activity during higher temperature processing of lead-free solders. In either case, it is important to ensure no residue is left that may interfere with the underfill process creating voids or adhesion issues. Lastly, it is important to choose a flux with an 8+ hour working life and that has sufficient tackiness to prevent the part from skewing during reflow. MEMS devices are extremely light weight and can be easily moved from the desired position.

Solder reflow profile selection and substrate metallization are of equal importance to the previous steps in achieving proper bump wetting and collapse. In an ideal scenario, it is desired to achieve a 15-30% collapse of the solder bump and have the solder completely wet the substrate surface. Examples of properly wet and non-wet bumps are provided in Figure 1.

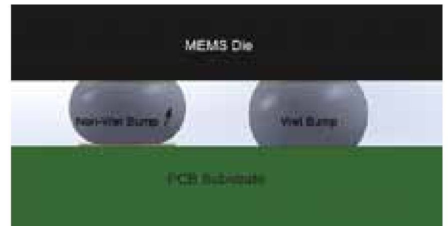

Figure 1. Non-wet and wet solder bumps.

A typical reflow profile for SAC 305 lead-free solder consists of pre-heating including soak, reflow and cool down zones. To achieve the proper wetting defined above for MEMS applications, the typical reflow profile needs to be adjusted. More specifically, it is important to minimize the preheat zone to keep the flux active and prevent it from drying out. This could result in nearly a straight ramp to the reflow zone. In addition, the reflow zone needs to be adjusted to compensate for the level of oxide on the bumps and type of solder being used. It's best to keep reflow peak temperature as low as possible while still maintaining a reasonable process window. If the reflow is performed in a nitrogen atmosphere, which is highly recommended to limit oxide growth, the peak temperature will be lower and the reflow zone shorter. If reflow is performed in air, one can expect higher reflow peak temperature for longer duration. Although a nitrogen atmosphere is recommended, it is not always easily implemented, especially when production equipment is already in place, or funds are extremely limited in a medical device startup. In other cases, the product may already be launched with an air reflow process with poor yield, and it could be weeks before an equipment upgrade to add nitrogen can occur. Figure 2 shows a typical lead-free solder reflow profile with two modified versions, for air and nitrogen, as described above.

After reflow is complete, underfill application is an important step to minimize the stress induced in the solder joints from differing coefficients of thermal expansion (CTE) of the substrate and MEMS flip-chip. The underfill minimizes shear forces on the bump and causes the substrate and chip to slightly bend as one unit. Another critical function of the underfill is to prevent tin whiskers from creating shorts between the bumps. Lead-free solders have a high percentage of tin and are highly susceptible to this unpredictable failure mode. NASA has observed whisker formation after a few hours, and in some cases, they do not form for many years [1].

A robust metallization for the bond pad on the mating substrate is also required to prevent oxide growth, ensure proper wetting and excellent adhesion. On printed circuit boards, this metallization is often electrolytic or electroless nickel with flash gold over a copper base layer. There are multiple

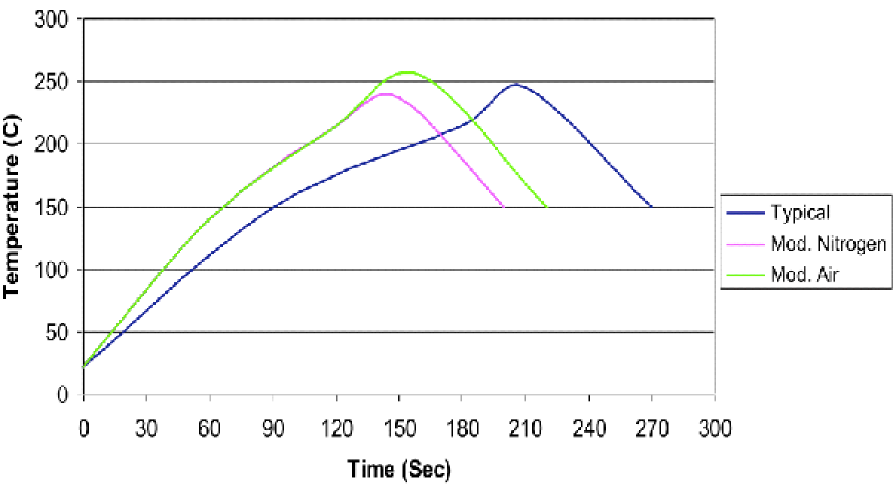

Figure 2. Typical and modified lead-free solder reflow profiles for SAC 305.

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options for the chip metallization, but one popular example is immersion gold over electroless nickel with a zincated aluminum base layer. Both Pac Tech and Uyemura have reported differing levels of success with palladium as a diffusion barrier between the nickel and solder. The tin and nickel intermetallic is brittle and can be a source of failure in high stress conditions such as drop test. There are examples of palladium use between the nickel and gold layers, or as the top layer without gold [2-3].

Summary

The difficulties in creating robust lead-free solder joints for medical MEMS flip-chip applications of increasing smaller size with confounding process parameters and materials is a real challenge. The solution to this problem lies within an intertwined mix of oxide growth minimization, proper material selection and application, and subtle process parameter adjustments. More specifically, cleanliness, proper storage and handling or pre-bake, flux and its application, the solder reflow profile, chip and substrate metallizations and underfill, are all critical elements in the process. Hence, when each of these parameters and materials are designed to work together, robust lead-free solder joints with high first-pass yields can be achieved.

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Biography

David DiPaola is Managing Director for DiPaola Consulting, www.dceams.com; email david@dceams.com

Ultratech Acquires Assets of Cambridge Nanotech, Inc.

Ultratech, Inc. has acquired the assets of Cambridge Nanotech, Inc. Based in Cambridge, Mass., Cambridge was a leader in atomic layer deposition (ALD) solutions with hundreds of system installations in research and manufacturing settings worldwide. Financial terms of the transaction were not disclosed. With this acquisition, Ultratech expands its nanotechnology and intellectual property (IP) portfolio with ALD technology to provide solutions for new layers within the electronics industry and entry into new markets, such as biomedical and energy.

The company noted that ALD technology will be in high demand in volume manufacturing environments, and in particular for micro-electro-mechanical systems (MEMS), implantable devices in the biomedical sector, and batteries and fuel cells in the energy arena. ALD is an enabling technology and provides coatings and material features with significant advantages to other existing techniques.

Ultratech Chairman and Chief Executive Officer Arthur W. Zafiropoulo stated, "As a global leader in experimental ALD solutions, Cambridge has developed a portfolio of valuable technology and systems. We plan to integrate the intellectual property acquired from Cambridge Nanotech into Ultratech and include the ALD systems in our nanotechnology product group. By increasing our IP and expanding our nanotechnology portfolio to new levels, we expect to generate a new revenue stream in existing and new markets."

A*STAR's IME Launches 2.5D Silicon Interposer Multi-project Wafer Offering

The Institute of Microelectronics (IME), a research institute of the Agency for Science, Technology and Research (A*STAR) in Singapore, announced the launch of its 2.5D through-silicon-interposer (TSI) multi-project wafer (MPW) service, aimed at providing a cost-effective platform to do research and development prototyping and proof-of-concept in 2.5D TSI technology.

Supported by IME's state-of-the-art 3D through-silicon-via (TSV) engineering line, the MPW service is a one-stop solution for 2.5D TSI R&D prototyping that comes with comprehensive design kits, via and redistribution/bumping technology, as well as packaging and assembly capabilities. By enabling the heterogeneous integration of different functionalities including logic, memory, analog/RF, photonics, micro-electromechanical systems, devices with more functionality, smaller form factor and less power consumption can now be realized.

The service will enable the academic, research and industrial community to develop 2.5D research test vehicles with leading-edge designs, materials and processes so that they can be applied to products such as smart phones, tablets, networking and sensors, and biomedical applications.

A*STAR's IME to Collaborate with SFC Fluidics® on Automated Biosensor

A*STAR recently announced that through its Institute of Microelectronics (IME), it will be collaborating with SFC Fluidics®, a USA microfluidics-based biomedical device development company, to develop a portable diagnostic tool for rapid triaging of traumatic brain injury (TBI) victims and to improve the treatment strategies. TBI is one of the most common causes of death and disability in the world, usually resulting from blasts, falls,

knocks, traffic accidents, and assaults.

The proposed diagnostic tool is a fully-integrated, automated biosensor device that requires only a drop of blood to detect up to three biomarkers released by the brain after sustaining injury. The biomarker readings will be displayed on an easy-to-read screen, along with an indicator, alerting the caregiver to the severity of the injury.

Unlike conventional diagnostic tools such as neurological tests and computed tomography (CT) scans, the biosensor device does not require any trained personnel for sample handling. The portable feature of the device facilitates rapid on-site diagnosis of the injury. Caregivers will be able to respond quickly with the proper course of treatment to prevent injury aggravation.

The biosensor device leverages and integrates IME's silicon-based microfluidic sensor and biosensor technology and bio-electrochemical assay development capability. IME has built up strong capabilities in biomedical microsystems and has established deep collaborations with the clinical community and key industry partners in Singapore to advance silicon-based point-of-care diagnostics devices.

SFC noted that, by leveraging IME's industry standard mass production facilities, the company will be able to cut down the product development cycle time. SFC's VP of R&D, Sai Kumar, stated that the TBI project is the start of a longer term collaboration that the company will explore together with IME.

AG Semiconductor Services Enters Remarketing Business

AG Semiconductor Services, LLC (AGSS), announced the formation of a new remarketing services division targeting 150, 200 and 300mm semiconductor, IC test/assembly and printed circuit assembly equipment. The company has made a significant investment in personnel and business systems to ensure its ability to deliver a full slate of remarketing services in addition to the purchase and sale of surplus semiconductor manufacturing equipment, turnkey solutions, inventory management, market metrics, compliance control, and the ability to reach the largest number of buyers. A seasoned team has been brought on board to ramp up the remarketing activities. The majority of the new remarketing team came to the company from the former GE Capital Global Electronics Services' (GES) remarketing business.

ZESTRON Opens Japan Headquarters and Technical Center

ZESTRON has opened its Japan Headquarters and 6th Technical Center located in Kanagawa; it represents the company's 4th Asian Technical Center.

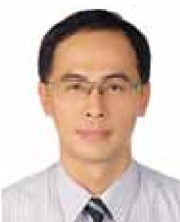
Figure: ZESTRON Japan Headquarters and Technical Center

The investment enables the company to introduce leading edge aqueous-based cleaning agents within this market as an environmentally sound alternative to the many solvent-based cleaning products currently used.

Mr. Daido Sawairi, General Manager for ZESTRON Japan, is responsible for operations and leading the local application engineers and sales team. He has over 20 years of domestic and international business experience in the electronics field and has held various management positions during his career.

Test Advantage Hardware Names Billy Liu Country Manager for Taiwan

Boston Semi Equipment LLC (BSE Group) announced the appointment of Billy Liu as Test Advantage Hardware's country manager for Taiwan. Liu is responsible for managing Test Advantage's expanding business for new and pre-owned semiconductor test equipment, spare parts, technical capabilities and financial solutions within Taiwan.



Billy Liu

Liu will work within the company¹s newly formed Taiwan operation, Test Advantage PTE Ltd., Taiwan Branch, with additional responsibilities for staffing and recruitment. He brings a background in semiconductor test and over 18 years of experience in the technology industry within Taiwan.

Philippe Wieczorek Named Minalogic's Software Director

Minalogic announced that Philippe Wieczorek has been named director of the Software Department. He will be responsible for coordinating and expanding Minalogic's software development activities, including projects that help cluster members integrate innovative software features in microelectronics and develop smart miniaturized products and solutions.

Philippe Wieczorek

Wieczorek most recently served as chief of staff of Hewlett Packard's Internal Sites Management Team (ISMT) in Grenoble. In that position, he focused on creating R&D activity and on ISMT's relationships with institutional players and academics. At HP, Wieczorek also was an innovation manager for the company's Communications and Media Solutions business unit, managing international projects.

Earlier in his career, Wieczorek worked in the network and telecommunication fields, where he held engineering

positions ranging from software development to engineering manager. He also worked for five years at Cap Gemini S.A. He holds an MS in computer science from McGill University in Montreal, Canada, and an engineering degree from INSA Lyon, France.

Patrick Boisseau, Head of Leti's Nanomed Program, Elected Chairman Of the European Technology Platform on Nanomedicine

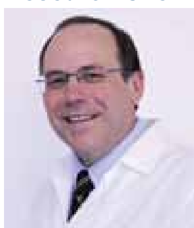
Patrick Boisseau

CEA-Leti has announced that Patrick Boisseau, the head of Leti's nanomedicine program, has been elected chairman of the European Technology Platform – Nanomedicine (ETPN), a joint initiative between industry, academia, clinicians and the European Commission to help build a profitable nanomedicine sector in Europe. Most of the innovation in Europe is occurring in research labs and small to midsize enterprises (SMEs), including start-ups that have spun off from universities and research institutes.

Boisseau said two of his primary goals during his two-year term as chairman of ETPN are keeping the nanomed innovation that is underway at many European facilities and SMEs in Europe, and to help build a nanomedicine sector that can compete strongly with Asia and the U.S. "One key way to do that is to organize a supply chain of SMEs to facilitate the transfer of innovation and technology to large companies and make these technologies available to patients as soon as possible," said Boisseau. "It also will require us to build key infrastructure in Europe, such as an EU nanotechnology characterization lab or a network of good manufacturing practices sites for medical nanomaterials. This initiative also will be a good opportunity for leading European institutes like KTH, EPFL, Helmholtz Foundation, Tecnalia, Fraunhofer, SINTEF, and Leti to expand their nanomed partnerships with both SMEs and large companies."

Boisseau has chaired the ETPN working group on nano-diagnostics since the ETPN was formed in 2005. In the same election, Dr. Laurent Levy, CEO of Nanobiotix, was elected vice chairman of ETPN. He represents SMEs on the platform's executive board.

Edward Watkins Joins SMT International as Senior Research Chemist



Edward Watkins

SMT International, LLC has just announced the hiring of Edward Watkins as a Senior Research Chemist for the company's AMTECH solder products. An accomplished chemist with decades of experience in research, product development and analytical testing, Mr. Watkins will utilize his extensive

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background and experience to assist in the development of innovative solder pastes, fluxes, and process support products utilized in circuits assembly.

Watkins' educational background includes degrees from Susquehanna University (BA) and Pennsylvania State University (PhD), as well as serving as a full-time associate research scientist at Yale University. Watkins' resume also includes working for global corporate leaders such as Pfizer, Dow Chemical and Amgen. These and other experiences have allowed Watkins to take a leadership role in product research and development, intellectual property rights and patents, technical writing, manufacturing and QC process development, regulatory investigations and filings, as well as managing teams of research scientists.

ESCATEC Promotes Markus Walther to CEO

Markus Walther

ESCATEC has announced the appointment of Markus Walther to the role of CEO of the ESCATEC Group, effective January 1, 2013. Markus started at ESCATEC as a Technical Manager 23 years ago and advanced through the company to his current role as COO. The position of COO will remain open until a suitable candidate is selected.

Christophe Albin, Executive Chairman of the Board of Directors and founder of ESCATEC, said, "Markus has made major contributions to the success of ESCATEC, helping the company establish itself as a major global player in the electronics engineering and manufacturing ("E2MS") industry through offering world class customer service backed by Swiss quality and reliability. It is particularly gratifying that our policy of continually investing in our people and their career development produces outstanding staff such as Markus, who has worked in most departments during his 23 year career at ESCATEC, and therefore has hands on experience to draw upon to bring out the best in people."

Commenting on his appointment, Markus Walther added, "I am very honored to continue to serve ESCATEC in my new appointment as CEO. Handing the day to day operational management of the business to a new COO will enable me to apply more of my time to supporting the strategic growth of the business. We see significant opportunities to grow through more focus on the US market, continuing to expand our presence in Europe, and offering a very effective manufacturing alternative in South East Asia to the ever increasing cost of China. It will also allow me to continue the development of, and investment in, our employees, our manufacturing technologies and capacity in order to support our growth strategy and with customer service always in our minds. We call this ESCATEC's way to success."

Barry Cox Joins Touchstone Semiconductor as Executive Chairman of the Board

Barry Cox

Touchstone Semiconductor appointed Barry L. Cox Executive Chairman of its Board of Directors. Cox brings more than 45 years of leadership experience in the semiconductor industry. He has held senior management positions including President, CEO and Chairman of the Board at several private and public corporations. In addition to Touchstone, he is a member of the Board of Directors of Pixelworks and Audience. He has served on the Board of Directors of 18 corporations and been involved in four public offerings, two secondary offerings and 11 acquisitions at these companies. He holds a Bachelor of Science degree from the US Air Force Academy and a Master's in Business Administration from Boston University.

Carsem Expands Role of VP Allan Calamoneri

Carsem announced that Allan Calamoneri has assumed the responsibilities of VP of Sales, North America, effective immediately. Calamoneri is based in the Scotts Valley, California office and reports to Albert Law, Carsem's VP of World Wide Sales and Marketing.

Calamoneri – who has a 23-year career in the semiconductor industry – has COO experience and a track record of successful results in both domestic and international management roles, noted the company. Associated with Carsem Inc. since 2004, his most recent experience was as VP of Test Business Development. In his new, expanded role, Calamoneri will have responsibility for the entire selling organization of Carsem in North America. Reporting to him are three regional sales directors and a technical sales director.

ECTC Registration is Now Open

This year's Electronic Components and Technology Conference (ECTC) will feature more than 300 high-quality papers over 36 oral sessions, four interactive presentation sessions and one student poster session.

The sessions cover peer-reviewed papers on 3D/TSV, embedded devices, LEDs, co-design, RF packaging, electrical and mechanical modeling, advanced packaging and interconnections technologies,

materials, assembly manufacturing, system packaging, optoelectronics, reliability, MEMS, and sensors.

There will also be four invited sessions:

LED Packaging Technologies and Market Trends – For A Brighter Future

Chair: Ricky Lee – Hong Kong University of Science and Technology

Packaging Challenges Across the Wireless Market Supply Chain

Chair: Lou Nicholls - Amkor

The Role of Wafer Foundries in Next Generation Packaging

Chair Sam Karikalan - Broadcom Corporation

CPMT Seminar: Advanced Low Loss Dielectric Materials for Large Data High-speed Wide Band Transmission

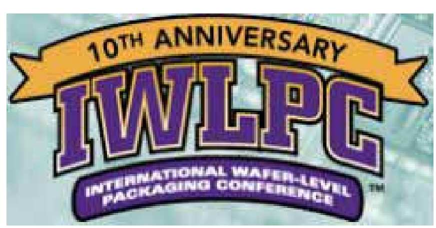
Chair: Kishio Yokouchi – Fujitsu ITL

And a special modeling session: Modeling and Simulation Challenges in 3D systems.

Chairs: Yong Liu - Fairchild Semiconductor; Dan Oh - Altera

The ECTC also features 16 CEU-approved professional development courses and over 70 exhibitors.

The 63rd ECTC, sponsored by the CPMT society of IEEE, will be held May 28 - 31, 2013 at the Cosmopolitan Hotel, Las Vegas, Nevada. For more information and registration, visit www.ectc.net.



Call for Papers International Wafer-Level Packaging Conference

The SMTA and *Chip Scale Review* are pleased to announce plans for the 10th Annual International Wafer-Level Packaging Conference and Tabletop Exhibition. This premier industry event explores leading-edge design, material, and process technologies being applied to Wafer-Level Packaging applications. There will be special emphasis on the numerous device and end product applications (RF/wireless, sensors, mixed technology, optoelectronics) that demand wafer level packaging solutions for integration, cost, and performance requirements.

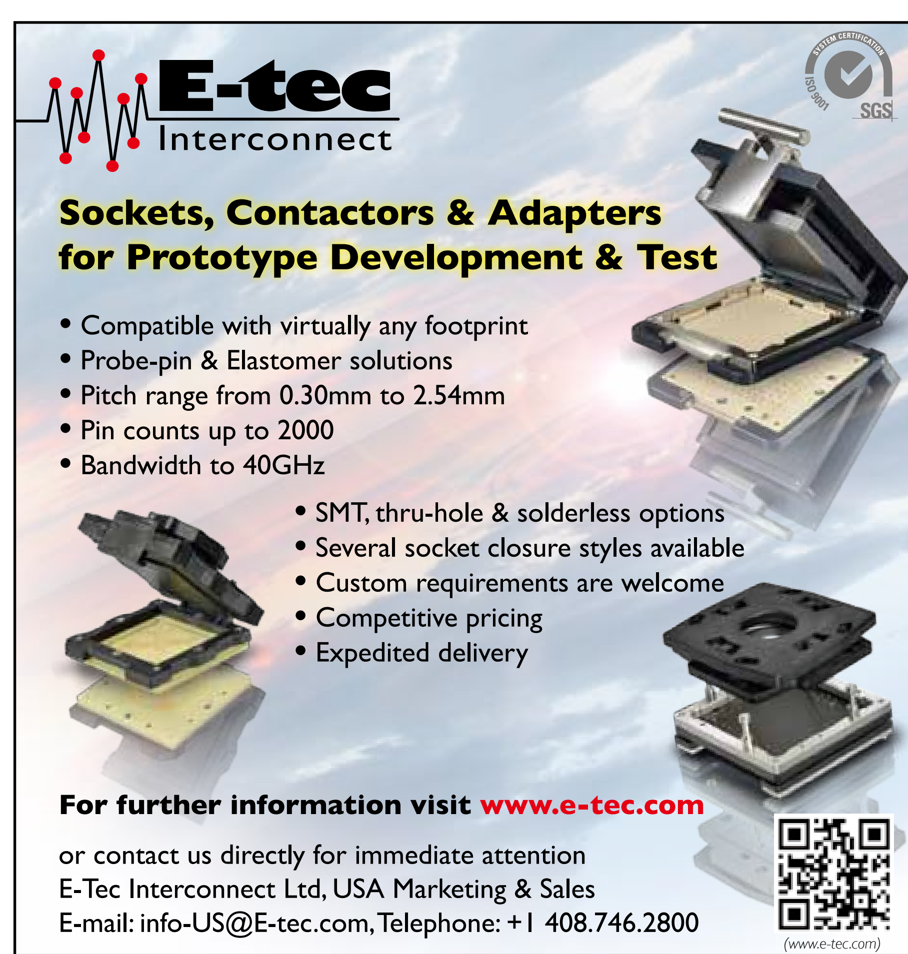
The IWLPC Technical Committee would like to invite you to submit an abstract for this program. **Abstract deadline is March 29, 2013.**

The conference includes three tracks with two days of technical paper presentations covering: Wafer Level Packaging; 3-D (Stacked) Packaging; and MEMS Packaging. Also we will offer professional development courses.

If you would like to present at this conference, please submit a 200-300 word abstract by March 29th, 2013. Please include a title, author name, and contact information with your abstract.

Note that technical papers are required and will be due August 23, 2013.

For more information on the conference, please contact Patti Hvidhyld at 952-920-7682 or to patti@smta.org. For information to exhibit and sponsorship opportunities please contact your CSR sales rep or CSR Publisher at info@chipscalereview.com



Cost Efficient Wafer-Level Stacking Technologies

By Mariam Sadaka, [Soitec USA] Ionut Radu, Chrystelle Lagahe-Blanchard, [Soitec France] Lea Di Cioccio [CEA-Leti]

3D integration aims at providing highly integrated systems by vertically stacking and connecting various materials, technologies, and functional components together. In this emerging field, new technologies and integration schemes will be necessary to meet the associated manufacturing challenges. To address these challenges, we have developed two wafer-level stacking technologies – Smart Stacking™ and Smart Cut™ – for improving the process cost efficiency and providing sub-micron alignment capability.

3D Process Integration Options

There are a number of 3D process integration options – the vertical stacking of top and bottom layers is one example. This stacking can be performed in two different ways: wafer-to-wafer (W2W) bonding, or die-to wafer (D2W) bonding. W2W bonding is where the entire top and bottom wafers are bonded together. D2W bonding is where the top layer is diced into chips that are individually stacked using pick-and-place on top of a bottom wafer. The bonding process for the two approaches is collectively performed in a single step. Dicing of the W2W stack is done through the entire bonded stack, whereas dicing for D2W is done through the bottom wafer with the bonded die on top.

With these two stacking options, different trade-offs arise. While D2W stacking uses known good die (KGD) and facilitates the integration of heterogeneous technologies, W2W stacking simplifies the stacking process flow and maximizes the process throughput for homogeneous technologies with matching die size. W2W bonding is a fab-compatible process with throughput independent of die size. D2W integration does not offer the same level of cleanliness when using standard wafer processing equipment, and wafer cycle time is directly impacted by die size [1]. W2W bonding is most suitable for applications with high wafer yield and matching die size; one example is memory stacking, which also benefits from a variety of repair strategies [2].

While there are still many remaining issues for 3D integration, cost is certainly a major challenge. We have developed a W2W high throughput direct bonding to improve process cost efficiency and to provide sub-micron alignment capability required for high-density through-silicon vias (TSV) [3]. This article will describe our building blocks for 3D IC wafer-level stacking: Smart Stacking – a high-throughput low temperature direct wafer bonding with sub-micron alignment, and Smart Cut – a low-temperature layer transfer stacking process.

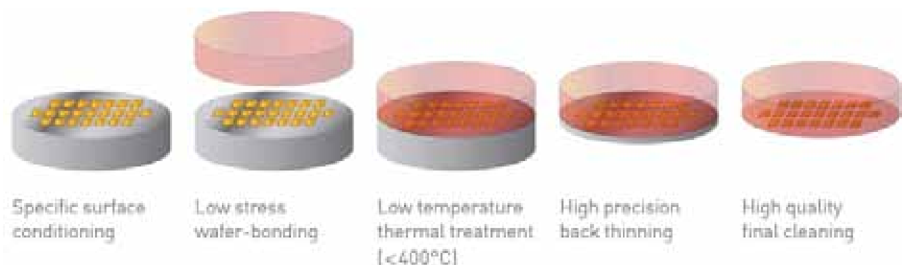


Figure 1a: Process schematic of the Smart Stacking technology.

Smart Stacking

Smart Stacking is a W2W stacking technology platform of partially or fully processed wafers (**Figure 1a**). The process includes surface conditioning, room temperature low stress bonding with alignment, low-temperature post-bond anneal, grinding and thinning. Room temperature bonding ensures low thermal expansion mismatch, less stress and mechanical deformation, which are critical for high alignment accuracy [4]. To address the thermal budget constraint imposed by stacking of backend of the line processed wafers (i.e., < 400°C), specific pre-bonding surface conditioning and a post-bonding thermal treatment were developed to control and increase the bonding strength within the reduced thermal budget window. High bonding energies where achieved thereby providing compatibility with aggressive wafer grinding and thinning processes [5, 6].

The low-temperature wafer bonding step includes dielectric bonding or patterned metal bonding. Dielectric bonding provides a mechanical bond and the metal bonding provides a mechanical as well as an electrical bond between the bonded wafers. Smart Stacking with dielectric or metal direct bonding exhibits a similar process throughput of 15-20 wafers/hr unlike other bonding processes, which could take up to 2-4 wafers/hr [7].

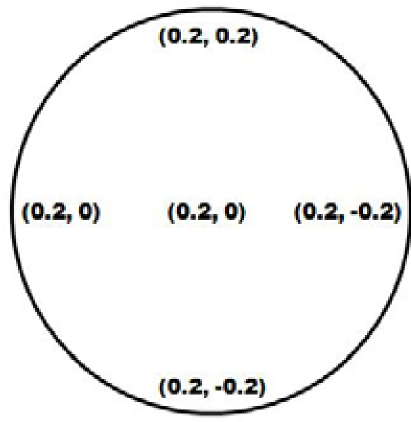


Figure 1b: W2W alignment accuracy across a 300mm wafer.

Precision W2W alignment represents a key requirement for the wafer-level vertical integration of 3D ICs. Following the preparation of the patterned surfaces, the processed wafers are bonded using an EVG Smartview® tool. The common alignment specification for this tool is ±1µm, and the alignment is measured using an infrared transmission microscope. Since no external force or pressure, or temperature cycle, is applied during the bonding process, excellent alignment with minimum mechanical deformation is obtained. W2W alignment accuracy of ~0.2µm across 300mm wafers has been achieved (**Figure 1b**) [5, 6].

Oxide-Oxide Direct Bonding

Smart Stacking technology based on low-temperature dielectric, hermetically sealed, and reliable (MIL-STD883) direct bonding, is a promising path for 3D integration that benefits from established oxide-oxide bonding technology [8]. The motivation behind dielectric bonding is to achieve a mechanical bond between the face-to-face (F2F) bonded wafers without introducing new materials in order to maintain manufacturability and reliability standards. This stacking process requires a TSV last approach to form the desired inter-wafer connection.

Direct bonding of two oxide surfaces requires considerable control of surface properties. The Smart Stacking technology was demonstrated on 300mm wafers with more than 10 layers of backend metal (10ML) and a deposited oxide layer on top acting as the bonding layer. Wafer topology was controlled by a chemical-mechanical polishing process that maintains wafer edge quality and wafer micro-roughness <0.5nm RMS. This process is fully compatible with common interconnect planarization capabilities [5]. It is demonstrated that with the appropriate choice of oxide and pre-bonding surface conditioning, high bonding energies can be achieved even after low temperature treatments. Low-temperature deposition of plasma-enhanced chemical vapor deposition (PECVD) silane-based oxides and dry plasma activation achieve surface energies $>1 J/m^2$ at only 200°C (**Figure 2a**). An acoustic microscope image of two bonded 300mm wafers with more than 10ML show excellent defectivity at the

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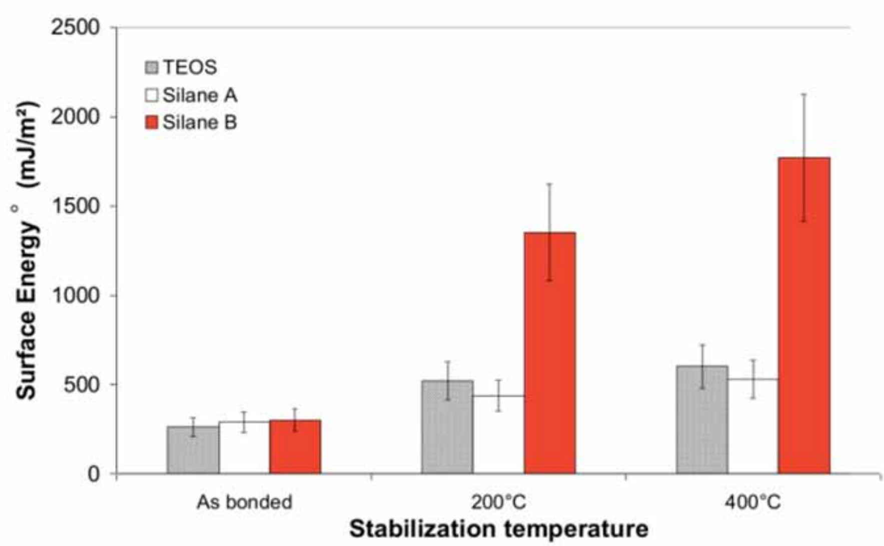

Figure 2a: Surface energy (γ) evolution with temperature of oxide bonding stacks using three different deposited oxides.

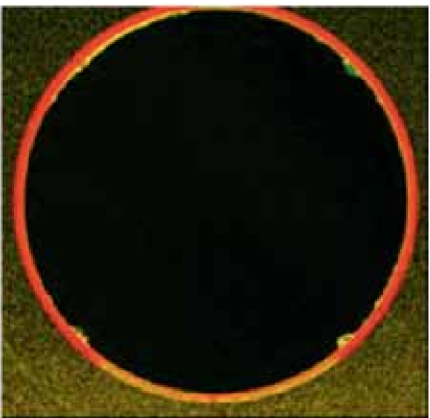

Figure 3a: Acoustic microscope image of the patterned Cu bonding interface (5x5µm Cu pad size and 10µm pitch, Cu density 20%) with 2h of annealing at 400°C

bonding interface and with minimum edge exclusion (**Figure 2b**) [5].

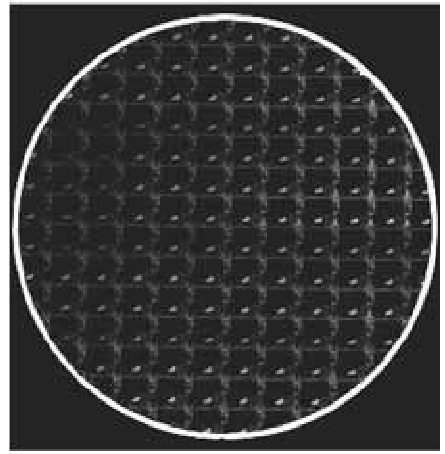

Figure 2b: Acoustic microscope image of the oxide bonding interface of 300mm processed wafers.

Metal-Metal Bonding

Smart Stacking technology based on low-temperature patterned metal bonding enables the formation of electrical connections during the stacking process—a promising path for high-density 3D interconnects [9]. Even if TSVs are still needed for power, input/output (I/O), and signal routing through the different strata, metal bonding has a significant bandwidth advantage over dielectric bonding [10].

Unlike thermo compression, the non-thermo compression bonding is performed at room temperature under atmospheric pressure and is based on molecular adhesion between surfaces in contact. The bonding process does not require any additional processing steps; standard dual-damascene processes and surface treatment techniques are optimized to ensure smooth hydrophilic surfaces for good bonding conditions [6]. The bonding can be done directly after standard backend processes and can be adapted with via middle and via last, F2F and F2B integration schemes.

Copper pad sizes varying from 5µm to 500µm with a pitch of 10µm and 40µm were investigated, and excellent bonding interface defectivity was demonstrated (**Figure 3a**). Typically, various interfaces are formed after patterned copper bonding. The bonding strength of the different types of interfaces has been evaluated (**Figure 3b**). The highest bonding energy is obtained for copper-copper (Cu-Cu) interfaces, followed by SiO_2-SiO_2. The Cu-SiO_2 interface leads to the weakest adhesion even after 400°C annealing [6]. Copper interdiffusion and/or grain growth across the Cu-Cu bonded interface are the driving forces for achieving high bond strength [6, 8]. The achieved bonding strength has been sufficient to sustain post-processing such as silicon back thinning using coarse and fine grinding. In terms of electrical characterization, a specific contact resistance of 0.5Ω•µm² for a 10x10µm² contact area after annealing at 200°C

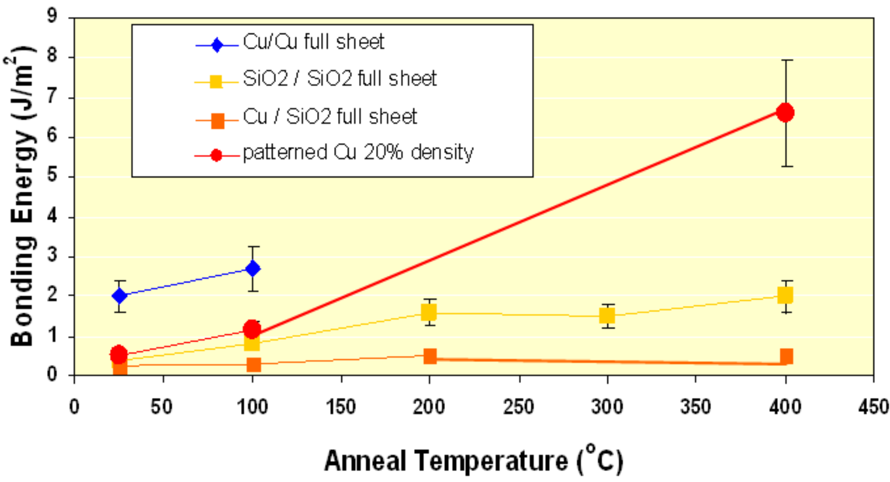

Figure 3b: Bonding energy evolution with temperature of different types of interfaces (Cu-Cu, Cu-Ox and Ox-Ox).

and 400°C for 2h was achieved [6, 11]. The resistance per node extracted from a ~30K daisy chain after 400°C post-bond anneal showed negligible resistance induced by bonding [11, 12]. In addition, initial reliability data based on electromigration (EM) testing shows that the bonded metallic interfaces are not the dominant path for the EM phenomena [13].

Stacking by Smart Cut

Smart Cut technology [14] provides a path to monolithic 3D integration and enables the transfer of a blanket layer of single-crystal Si film onto a processed wafer (**Figure 4a**). On this new single-crystal Si surface, a second level of devices can be processed and this integration can be repeated in an iterative mode.

This technology benefits from existing high-volume manufacturing SOI infrastructure in addition to optimum donor wafer recycling techniques for lower cost-of-ownership.

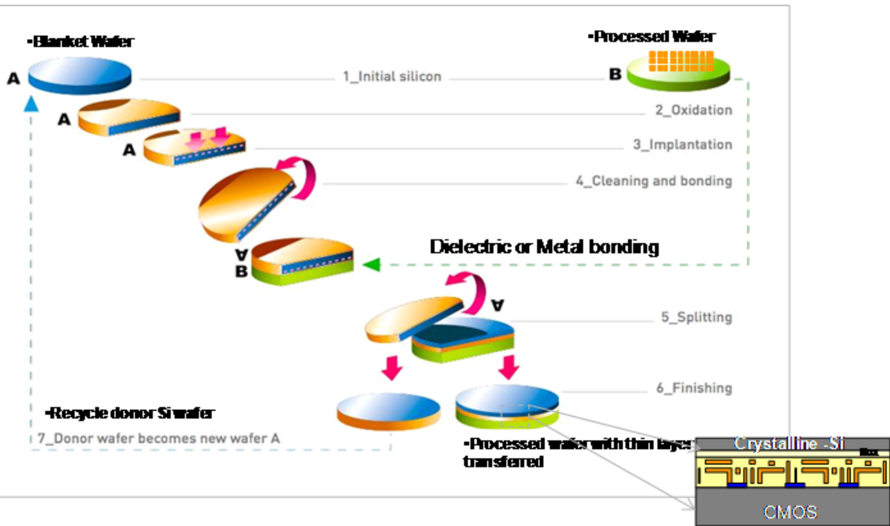

Figure 4a: Process schematic of the Smart Cut Technology

Compared to standard back thinning techniques, the Smart Cut atomic level splitting enables ultrathin (down to 0.1µm) layer transfer, thus simplifying and lowering the cost-of-ownership of the TSV process. The ultrathin transferred Si contributes to a smaller TSV aspect ratio that allows scaling to a higher TSV density, or simply the use of more cost effective regular backend vias instead, thus making this technology attractive for applications that require higher interconnect densities.

This approach is based on our ability to optimize the bonding energy by diminishing the overall thermal budget

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(as done for Smart Stacking) as well as optimizing the splitting kinetics to achieve splitting at low temperature (<350°C) [5,15]. The transfer of the 200-400nm ± 15nm top layer was demonstrated on a 300mm patterned wafer with low surface micro-roughness [8,16] (**Figure 4b**). The throughput of this process is slightly higher than the Smart Stacking process (~20-25 wafers/hr) because stacking by Smart Cut does not require critical alignment. Devices formed on the new Si surface on top of the processed wafer will be constrained by the thermal budget limitation of the handle processed wafer.

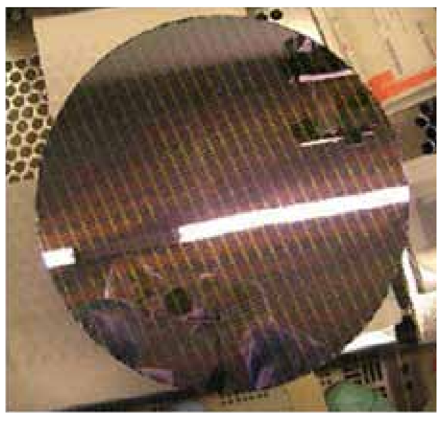

Figure 4b: 300mm Si layer transfer demonstrated on patterned wafers (200nm ± 15nm transferred layer, RMS ~1.2Å 2x2μm^2).

Summary

Smart Stacking and Smart Cut wafer-level stacking technologies provide high-throughput processes contributing to improving the overall stacking process cost-of-ownership. Smart Stacking is a key technology for realizing high-throughput dielectric or metallic direct bonding at low temperature, no applied pressure, and with critical sub-micron alignment. We have shown high quality dielectric direct bonding as a promising path for 3D integration that benefits from established oxide-oxide bonding technology. We demonstrated Cu-Cu non-thermo compression direct bonding with sub-micron alignment as a promising path for high-density low-resistance 3D interconnects. We further illustrated the transfer by Smart Cut of a blanket layer of single-crystal Si film on a processed wafer suitable for 3D monolithic integration; this is an integration scheme well-suited for applications that require higher interconnect densities.

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Biographies

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Lea Di Cioccio received a PhD in material and semiconductor physics from the Institut National Polytechnique de Grenoble, France; she is a specialist in semiconductor heterostructures and 3D integration at CEA-Leti.

A PoP for the Post-PC Era

By Ilyas Mohammed [Invensas Corporation]

Mobile computing has evolved beyond PC computing capabilities and can carry out tasks ranging from office productivity and communication to high-density (HD) media and gaming. There are three broad trends in computing over the past few years that have a significant impact on the processor-memory architecture and its implementation. They are: 1) The transition from single core to multi-core CPUs, which dramatically increased the need for multiple memory channels, the channel bandwidth and the amount of memory that is accessible to each core; 2) Low power computing that emphasizes physically short interconnects along with a wide bus at lower speeds for high bandwidth, and 3) Cloud computing, which benefits from having both hardware and software optimized and centrally managed for power and usage.

The most critical feature to keep increasing the performance is the processor-memory interconnect. The CPU and memory cycle time gap is increasing, which means that it takes far longer to get data to the processor than the time taken to use it. This problem is typically addressed by optimizing across various memory hierarchies. Knowing that storage is not suitable due to its very high latency, processor-DRAM subsystem receives the most attention for improvement.

Hence, there is a need for a solution that addresses the processor-memory bottleneck through very wide I/O for high bandwidth while consuming low power. An order of magnitude increase in the processor-memory I/O will make the 3D package a universal candidate for high computing. The current package-on-package (PoP) modules have limited data I/O (~32-64) and a new technology is needed to meet the high I/O (128-512) requirements. Bond Via Array™ (BVA™) Package-on-Package (PoP) offers ultra-high bandwidth between multi-core CPU-GPU SoC processors and wide I/O low power memory chips utilizing conventional wire-bond technology and existing materials and infrastructure.

Bond Via Array (BVA) Package-on-Package (PoP)

Figure 1 illustrates the Bond Via Array (BVA) wire-bond array interconnect concept. The main feature is that the BVA interconnects (free-standing wire-bonds) extend from the bottom substrate to the top surface of the bottom package to be connected to a package mounted on top.

The mature wire-bonding technology offers very fine pitch, and free-standing wires are formed using proprietary processes utilizing conventional wire-bond equipment. As the wire-bonds can be done at a pitch as small as 50µm, and can extend in length to any desired value, high aspect ratio (height to diameter ratio greater than 10) interconnects can be achieved. This interconnect technology lends itself to a wide variety of 3D packaging, including PoP, wafer level, embedded, etc.

The interconnect scaling capabilities are tabulated in **Table 1**. For a given 14mm x 14mm package and assuming a 1mm peripheral width for I/O, up to 1440 interconnects can be formed at 0.2mm pitch. These numbers of I/O are enough to meet future wide I/O memory requirements.

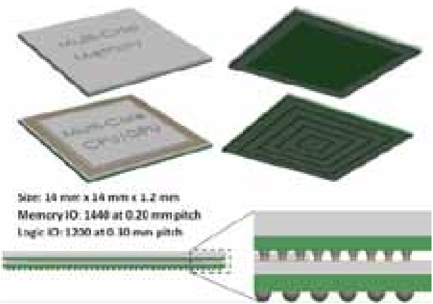


Figure 1: BVA PoP design features.

Manufacturing Process

A 432 I/O BVA PoP daisy-chain test vehicle was designed and fabricated that measured 14mm x 14mm with two perimeter rows of palladium-coated copper wires at 0.24mm pitch with a wire diameter of 50µm and a height of 0.4mm. This test vehicle has an interconnect aspect ratio (height/diameter) of 8 and pitch ratio (height/pitch) of 1.7, which is better than any existing PoP technology.

The process flow for the BVA PoP consists of stacking a memory package over a logic package with BVA interconnects. The top (memory) package is similar to current memory packages, including high I/O BGA. For example, four memory chips with each being x32 can be packaged to form a x128 BGA package. With higher I/O, wide I/O memory can also be used. The bottom package has the logic device

		No. of interconnect rows				
Pitch (mm)		2	3	4	5	6
	0.50	200	288	-	-	-
	0.40	248	360	-	-	-
	0.30	336	492	640	-	-
	0.25	408	600	784	960	-
	0.20	512	756	992	1220	1440

Table 1: Maximum possible interconnects as a function of pitch.

in conventional flip-chip format, with the BVA wires around the periphery. The molding with wires is also different. Finally, stacking is done using conventional surface mount technology (SMT) with the condition that the top memory package has fine pitch BGA. The four unique process steps are explained below.

Forming the BVA Copper Interconnect. The free-standing wire-bonds are the most important feature of BVA PoP. Forming the wire-bonds with the tips having good positional accuracy (x and y) and uniform height (z) are important in enabling very fine pitch and high yield package assembly. Figure 2 shows bottom package substrate with the flip-chip attached logic chip and BVA around the periphery.

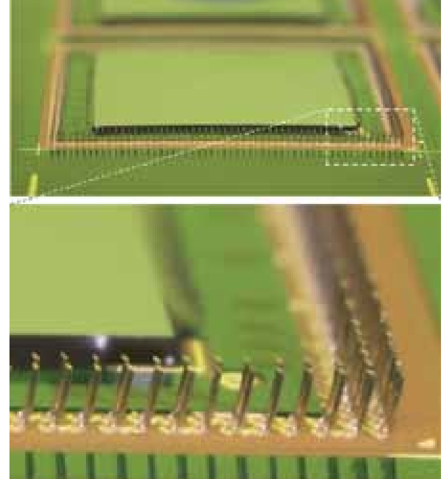


Figure 2: BVA interconnects (free standing wire-bonds) at 0.24mm pitch around the periphery of the bottom (processor) chip.

The x, y and z positional accuracy data is shown in Figure 3. The results given in these graphs depict data from 43 packages with each data point on the graph representing all the wire bonds in one package. The average data is within 20µm for all x, y and z positions, which translates to better than ±10µm. The wires were also bonded well, and an average of greater than 15 grams was obtained from bond pull test.

Molding and Exposing the Interconnect. The next step is to mold the logic package while exposing the BVA tips with a consistent desired height. A film-assisted mold technique was used to expose the tips. It is a mature technology commonly found in many packaging assembly operations and stable supplier support. The process uses a mold chase design with mold cavities only slightly deeper than the formed Cu wires. When the mold is clamped to the substrate, the Cu wires are pushed into the mold film. The mold cavity is filled with the molding compound, the molding compound is cured, the mold is opened and the mold film is pulled away from the package exposing the wire tips. The mold film thickness determines the wire tip exposure. Some process development was needed to optimize the wire tip exposure. No special molding parameters were needed to provide repeatable wire tip exposure results. The target value was 0.12mm and this height was obtained within a tolerance of ±10µm.

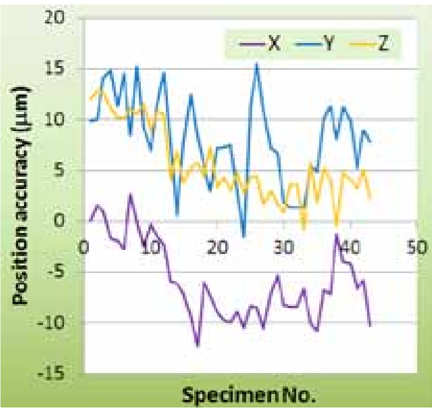
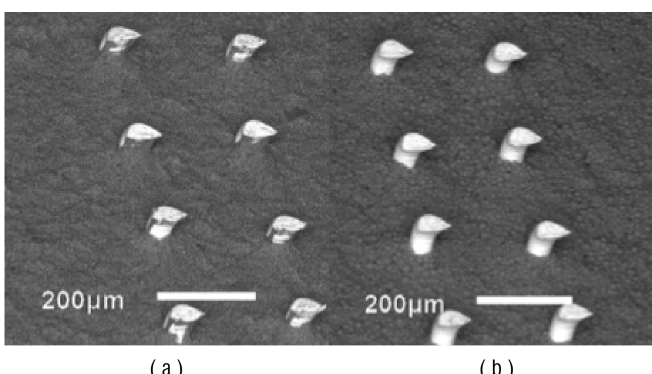


Figure 3: Wire-bond tip measured position data.

Cleaning wire tips with Robust Surface Finish. The wire tips need to be cleaned after molding and various techniques such as wet blast and chemical etch were used. The best results were obtained with wet etch as shown in Figure 4. The exposed wire height increased uniformly by about 10µm because of this cleaning step.



(a) (b)

Figure 4: Wire tips a) before and b) after wet etch.

Connecting Top Package to Exposed Wire Tips. The last step is to stack the memory package on top of the logic package, as shown in Figure 5. This process is very similar to conventional PoP assembly where solder paste is printed on the main board, the logic package is placed on the board, the memory package is dipped in solder flux and placed on top of logic package, and the stack is reflowed along with other components on the board. An underfill may be dispensed along the periphery of the stack for high reliability under dynamic loading. Good joints were obtained across all interconnects over the whole package, as shown in Figure 6.

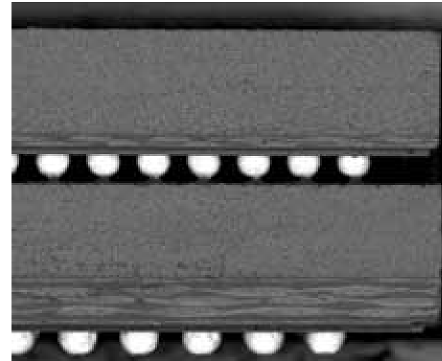


Figure 5: Assembled BVA PoP.

Reliability

A full suite of reliability tests were done and the results are summarized in Table 2. The moisture sensitivity level (MSL) 3 test was done for individual memory and logic packages. The high temperature storage and unbiased autoclave tests were done as PoP (memory package stacked on logic package) with underfill between them. The board level thermal cycling and

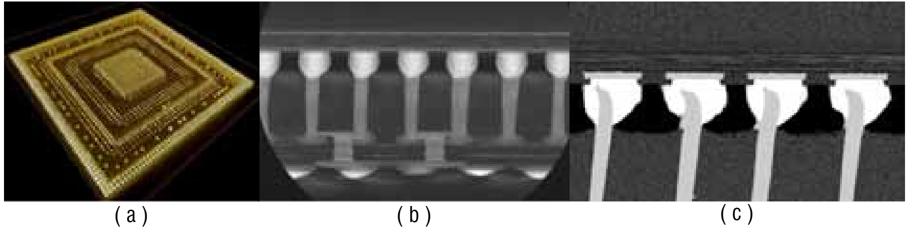


Figure 6: a) 3D CT scan image of the BVA PoP; b) 2D CT scan image of the BVA interconnect; and c) SEM image of the BVA to solder joint cross section.

drop tests were done with PoP on the test board with underfill. The underfill was used for all cases since this is a common implementation in phones and other mobile devices. All the tests passed without any failures. The drop test was extended up to 128 drops before stopping the test and no failures were detected.

To study the effect of copper-tin diffusion between the copper wire and the solder ball, accelerated testing was done by evaluating the amount of intermetallic formation under high temperature storage test (3x solder reflow cycles followed by 230 hours at 175^{0}C). To inhibit diffusion and intermetallic formation, the copper wires were coated with palladium. **Figure 7** shows that wet etch method has not damaged the wire tip palladium coating, which has served as an effective barrier against intermetallic growth, whereas the wet blast method has damaged the coating leading to extensive intermetallic growth.

Summary

Mobile computing requirements driven by multi-core, low power and cloud computing trends have placed a high premium for high processor-memory bandwidth through a very large number of interconnects with short physical length. To meet this challenge, an interconnect technology is presented that is based on wire bonds and can be utilized in different applications such as 3D packaging, embedded packaging,

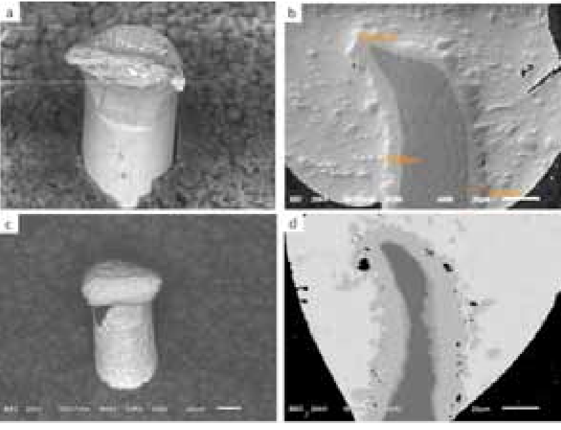


Figure 7:The wet etch cleaned wire tip a) before and b) after high temperature storage test, and the wet blast cleaned wire tip c) before and d) after high temperature storage test.

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Test	Standard	Test condition	Sample size	Evaluation	Result
Moisture sensitivity Level 3	IPC/JEDEC-J-STD-020C	125^{0}C for 24hrs; 30^{0}C/60% RH for 192 hrs, 3X Pb-free reflow	22 logic and 22 memory packages	C-SAM inspections at T0 and post-MSL3	Pass
High temp. storage	JESD22-A103D-condition B	150^{0}C, 1000 hours	22 PoP off-board	E-test after 168, 500 and 1000 hours	Pass
Unbiased autoclave	JESD22-A102D-condition D	121 C/100%RH/2atm for 168 hours	22 PoP off-board	E-test after 96 and 168 hours	Pass
Drop test	JESD22-B111	>30 drops, 1500 G, 0.5 msec of half sine pulse	20 PoP on board with underfill	In-situ monitoring	Pass (128 drops)
Temp. cycling (board level)	JESD22-A104D Condition G	MSL3 and then -40 ^{0}C to 125 ^{0}C , 1000 cycles	45 PoP on board with underfill	In-situ E-test up to 1000 cycles	Pass

Table 2: Current status of BVA PoP qualification testing.

wafer-level packaging, etc. The key benefits of this technology are as follows:

High performance. Ultra-high I/O (quad-channel+) between the bottom logic package and the top memory package offers a greater than 12.8GB/s bandwidth through a >1000 logic to memory interconnects package at a 0.2mm pitch in a standard 14mm x 14mm package.

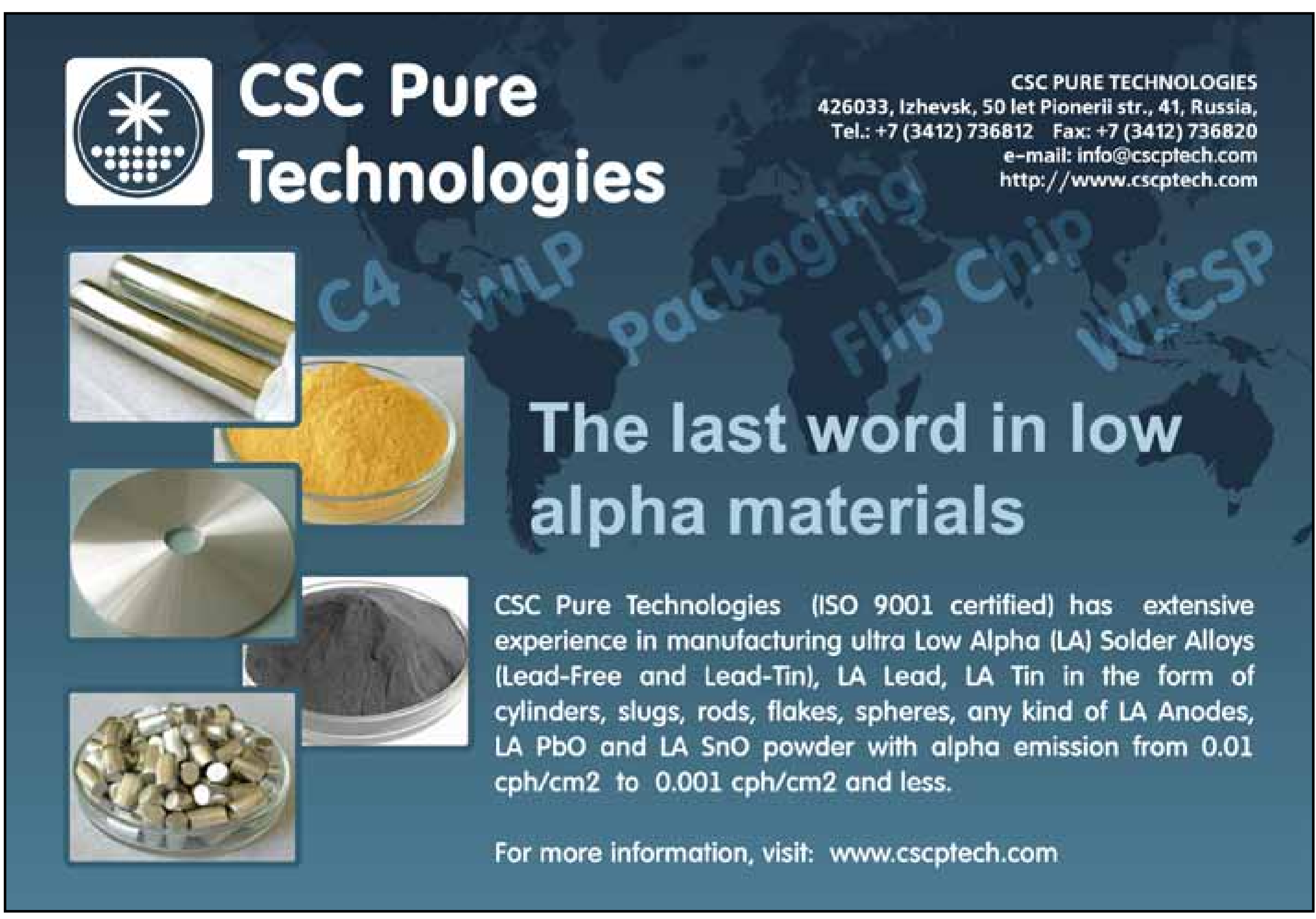
PoP approach. This approach has been independently sourced, packaged, and tested logic and memory for high yield and supply chain flexibility

Memory compatibility. The technology uses current LPDDR2 and LPDDR3, while being scalable to wide I/O memory devices

High-level package reliability and low cost. The method uses established assembly equipment, processes and materials with completely molded top and bottom packages for low warpage and standard SMT for high yield.

Biography

Ilyas Mohammed received his PhD from the U. of Texas at Austin and a BTech from the Indian Institute of Technology, Madras, India, both in aerospace engineering. He is a Sr. Director and Principal Technologist at Invensas Corporation; email imohammed@invensas.com



Supply Chains for High-Volume Manufacturing of 3D IC Integration

By John H. Lau [ITRI]

3D IC integration is taking the semiconductor industry by storm. It has been: (a) impacting the chip suppliers, fabless design houses, foundries, integrated device manufacturers, outsourced semiconductor assembly and test, substrates, electronic manufacturing service, original design manufacturers, original equipment manufacturers, material and equipment suppliers, universities, and research institutes; (b) attracting the researchers and engineers from all over the world to go to conferences, lectures, workshops, panels, forums, and meetings to present their findings, exchange information, look for solutions, learn the latest technologies, and plan for their future; and (c) pushing the industry to build standards, ecosystems and infrastructures for 3D IC integration.

This is a perfect storm! People and companies think that Moore's Law is going to take a bow soon and 3D IC integration is the next one. In order to prepare for their future and have a competitive edge, they have been investing heavily on both human and physical resources for 3D IC integration.

The potential applications and high-volume manufacturing (HVM) of 3D IC integrations is shown in **Figure 1** [1]. Basically, it can be classified into four groups, namely: memory-chip stacking, wide I/O memory (or logic-on-logic), wide I/O DRAM, and wide I/O interface (or 2.5D IC integration).

Memory-Chip Stacking

The drawing and sample in the far-left of **Figure 1** show the simplest example of memory-chip stacking published by Samsung in 2006. These chips could be DRAM (dynamic random-access memory) or NADA Flash with less than 100 I/Os (78 to be exact). Even with eight-chip stacking, their total thickness (560µm) is still less than that of an ordinary chip (this is significant). This memory-chip stack is attached to an organic substrate. Unfortunately, due to cost issue and competing wire bonding technology, memory-chip stacking with TSVs is not in volume production today for consumer products. Currently, Samsung is shooting for the next-generation server products and most likely is considering going with the DDR4 (double data rate – type 4) SDRAM (synchronous DRAM).

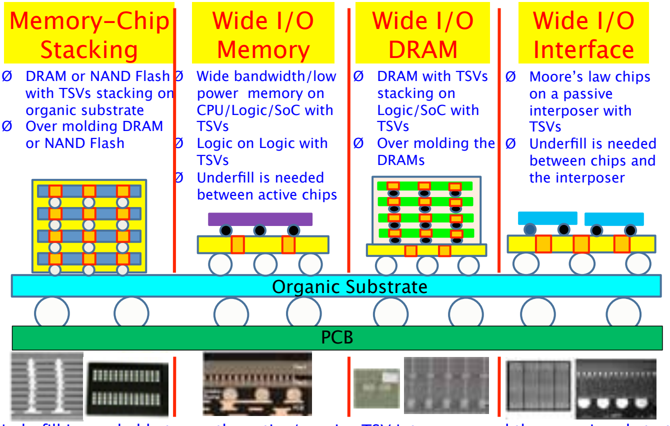


Figure 1: Potential applications and high-volume manufacturing of 3D IC integration.

Wide I/O Memory or Logic-on-Logic

The second column on the left-hand side of **Figure 1** shows a wide I/O memory, which consists of low-power consumption and wide-bandwidth memory usually with more than thousands of interface pins. This memory is supported by a CPU/logic or SoC with TSVs, which is called an active interposer. This wide I/O memory module is attached to an organic substrate. Since mobile products such as smartphones want it, samples have been made and published by, for example, Samsung. Unfortunately, the readiness of the fabless supply chain infrastructure, including industry standards, supply chain business models, and competitive pricing, takes time and is not here yet! Logic-on-logic falls into this category.

Wide I/O DRAM (HMC)

The third column on the right-hand side of **Figure 1** shows a wide I/O DRAM. Samsung has been publishing many papers on this topic for at least three years [2] and finally, at the 2011 IEEE ISSCC in San Francisco, the company showed the sample of two DRAMs on a master controller logic chip (or SoC) with TSVs, which is called an active interposer. For this DRAM, the number of TSVs and interface pins is slightly more than one thousand. The JEDEC standard defines this structure as having 1200 I/O pins in four channels (http://www.jedec.org/). This wide I/O DRAM module is attached to an organic substrate. Recently, the Hybrid Memory Cube (HMC) consortium, which includes such companies as Micron,

Samsung, Altera, ARM, Hewlett-Packard, IBM, Microsoft, Open-Silicon, SK Hynix and Xilinx, announced that a specification will be opened to the public by the end of this year. The specification is primarily targeted at high-performance networking, industrial, and test and measurement applications. IBM has also suggested it will use the cubes for high-end servers.

Wide I/O Interface with Passive Interposers (2.5D IC Integration)

The far right-hand side of Figure 1 shows a wide I/O interface for router/telecommunication/next-generation servers/high-performance applications. The Moore's Law chips (i.e., without any TSVs) have memory/ASIC/CPU/… and the I/O could be between hundreds and thousands, which are supported by a piece of silicon with TSVs and redistribution layers (RDLs). The sample in Figure 1 is presented by Xilinx [3-6], where the FPGA (field-programmable gate array) is fabricated by TSMC's 28nm process technology and the interposer is at 65nm. There are four RDLs on top of the interposer that lets those four FPGAs communicate to each other over very short distances.

The technology supply chains for these four groups of potential applications and HVM of 3D IC integration are discussed below. The thickness of the memory-chip stacking and DRAMs in the HMC is 50μm. Also, the thickness of the active and passive interposers is 200μm. Only chip-to-wafer (C2W) bonding is considered (supporting supply chains, such as materials and equipment, will not be mentioned). Though EDA (electronic design automation) supply chains are very important, they are not discussed in the present study. Vertically integrated companies such as Samsung and TSMC, which want to be the technology supply chain (i.e., do it all), also will not be discussed in this study.

Technology Supply Chains Before the TSV Era

Before the TSV era, the technology supply chains are very well defined and understood. Descriptions of the various entities comprising the supply chain before the TSV era are presented below:

FEOL (front-end-of-line). This is the first portion of IC fabrication where the individual devices such as transistors or resistors are patterned. This process is from a bare wafer to (but not including) the deposition of metal layers. FEOL is usually performed in semiconductor fabrication plants (fabs).

BEOL (back-end-of-line). This is the fabrication in which active devices are interconnected with wiring on the wafer. This process starts from the first layer of metal to bonding pads with passivation. It also includes insulators and metal contacts and is called MOL (middle-of-the-line). The term "MOL" is seldom used and embedded in the BEOL. Again, BEOL is usually performed in the fab.

OSAT (outsourced semiconductor assembly and test). This term is also called packaging, assembly and test. The process starts when the passivated wafer is received from the fab and then goes through circuit probing/bumping/thinning/dicing/wiring bonding/flip-chip/molding/ball mounting/final testing.

Technology Supply Chains for the TSV Era

The topic of supply chains in the TSV era will be discussed in three parts: A) Who makes the TSV? B) Who does the MEOL? C) Who performs the critical steps (including FEOL, MOL, BEOL, TSV, MEOL, assembly and test) and their ownership for making these four groups of 3D IC integrations shown in Figure 1.

A) Who Makes the TSV. The following steps in the TSV fabrication process impact the various considerations that must be addressed:

TSVs Fabricated by the Via-First Process: The TSVs are fabricated before the FEOL. This can only be done by the fab. However, even in the fab, this seldom happens because the devices (e.g., transistors) are much more important than the TSVs.

TSVs Fabricated by the Via-Middle Process: The TSVs are fabricated right after the FEOL (e.g., transistors) and MOL (e.g., metal contacts), and before the BEOL (e.g., metal layers), for example [7, 8]. In this case, the MOL is no longer embedded in the BEOL because the TSV fabrication process is between them (Figures 2 and 3). Owing to logistics and equipment compatibilities, usually the TSV by the via-middle process is done by the fab.

TSVs Fabricated by the Via-Last (From the Frontside) Process: The TSVs are fabricated (from the frontside of the wafer) after the FEOL, MOL, and BEOL. As of today, there is not a single paper published with this process.

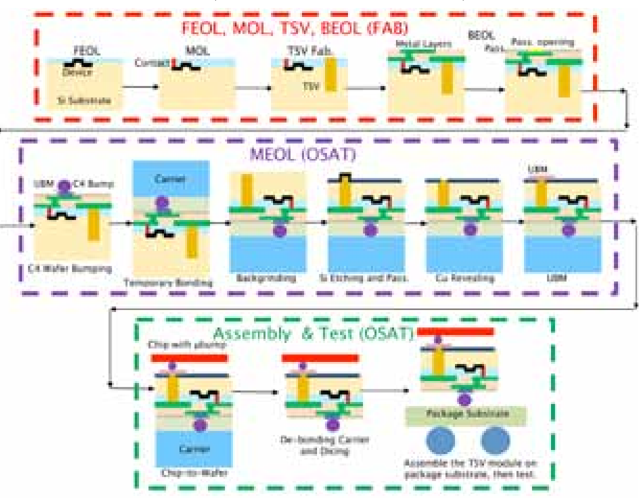


Figure 2: Critical steps and ownerships for (face-to-back) wide I/O memory using the TSV via-middle fabrication process.

TSVs Fabricated by the Via-Last (From the Backside) Process: The TSVs are fabricated (from the backside of the wafer) after the FEOL, MOL, and BEOL process flows. The CMOS image sensor is an example. Strictly speaking, CMOS image sensors are not examples of 3D IC integration. For CMOS device wafers, the only creditable publication is given by LETI, et al., [9]. However, due to logistics and technical issues, which will be discussed below, TSVs

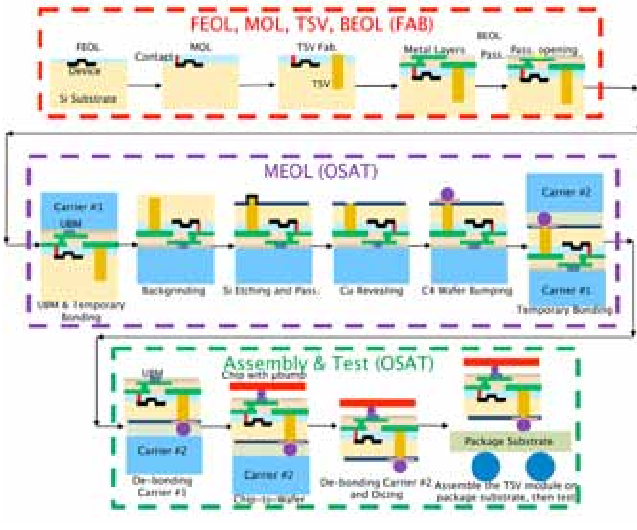


Figure 3: Critical steps and ownerships for (face-to-face) wide I/O memory using the TSV via-middle fabrication process.

fabricated by the via-last (from the backside) process should be avoided until these issues are resolved.

Based on the above discussions, it seems that for active device wafers being used for 3D IC integration applications, TSVs are better fabricated using the via-middle process. Also, the TSVs should be fabricated by the fab, where all the equipment and expertise already exist and the cost to fabricate the TSVs is less than 5% of the cost in fabricating the (32nm) device wafers!

How About the Passive TSV Interposers: When the industry defined the TSV processes for 3D IC integration, there were no passive interposers yet. Also, since there is no active device in the passive interposers, they don't fit into any of the preceding categories!

Who Wants to Fabricate the TSV for Passive Interposers: Both the fab and OSAT want to do it! It depends on the layout, design, and fabrication capabilities, especially the line width and spacing of the RDLs. Usually, a few microns of line width and spacing can be done by the OSAT. Otherwise, it should be done by the fab.

B) Who Does the MEOL. For the thicknesses of memory-chip stacking and DRAMs in HMC, and active and passive interposers under consideration, all the TSVs fabricated are blind vias. The blind TSV wafer is followed by solder bumping/temporary bonding/back grinding/TSV revealing/thin wafer handling/debonding/cleaning, which, taken together, are called MEOL (middle-end-of-line). In this study, except for the vertically integrated companies (e.g., TSMC and Samsung), it is better for the MEOL process flow to be performed by the OSAT.

C) Critical Steps and Ownerships for HVM of 3D IC Integration.

C.1) Wide I/O Memory (Face-to-Back) by the TSV Via-Middle Fabrication Process: Figure 2 shows

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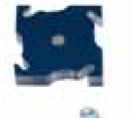
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the critical steps and ownerships for this process. After FEOL (to pattern the devices) and MOL (to make the metal contacts), the TSVs are fabricated by five key steps, namely via formation by deep reactive ion etch [10], dielectric deposition by plasma enhance chemical vapor deposition, barrier and seed layer by physical vapor deposition, Cu-filling by electroplating [11], and chemical mechanical polishing (CMP) to remove the overburden Cu [12]. These steps are then followed by the build up of the metal layers, and finally, the passivation/openings (BEOL). All these steps should be done in the fab.

The MEOL starts off by under bump metallization (UBM) and C4 ordinary wafer bumping with solder to the whole wafer. It is followed by temporary bonding of the TSV wafer to a supporting (carrier) wafer with adhesive [13, 14]. The next step is back grinding of the TSV wafer to a few microns from the tip of the Cu-filled TSV. This is followed by silicon dry etching to a few microns below the tip of the Cu-filled TSV. After that, a low temperature isolation SiN/SiO_2 deposition is applied to the whole wafer. Then CMP is used to remove the SiN/SiO_2 and the Cu and seed layers of the Cu-filled TSV (Cu revealing) [12, 15]. Finally, a UBM is built on the tip of the Cu-filled TSV. All these steps should be done by the OSAT.

Separately, the memory wafer is micro bumped with tiny solder bumps [16] or Cu-pillars with solder caps [17]. Then the wafer is diced into individual chips with micro bumps/Cu-pillars. These steps also should be done by the OSAT.

Next is chip-to-wafer (C2W) bonding [18, 19], i.e., the micro bumped memory chip is bonded (either by natural reflow or thermal compression) to the TSV wafer with the carrier. After face-to-back C2W bonding, the carrier wafer is debonded from the TSV wafer. It is followed by dicing the TSV wafer into individual TSV modules. This TSV module is solder (natural) reflowed on a package substrate, then tested. All these C2W bonding, dicing, assembly, and testing steps should be done by the OSAT.

C.2) Wide I/O Memory (Face-to-Face) by TSV Via-Middle Fabrication Process: The FEOL, MOL, TSV, and BEOL processes are exactly the same as those done in the TSV via-middle (face-to-back) process. However, the processes that follow it are different. Instead of C4 ordinary wafer bumping with solder after the UBM, the TSV wafer is temporarily bonded to carrier #1. Then, back grinding of the TSV wafer is done and the Cu reveal and UBM are accomplished. Those steps are followed by C4 ordinary wafer bumping with solder and temporary bonding to a second carrier #2. Then carrier #1 is debonded from the TSV wafer and C2W (face-to-face) bonding is performed. After C2W bonding, the carrier #2 is debonded from the TSV wafer. It is followed by dicing the TSV wafer into individual TSV modules. This TSV module is solder reflowed on a package substrate, then tested. The critical steps and their ownerships are shown in Figure 3.

C.3) Wide I/O Memory (Face-to-Back) by TSV Via-Last (from the Backside) Fabrication Process: Figure 4 shows the critical steps and their ownerships. After FEOL (to pattern the devices), MOL (to make the metal contacts), and BEOL (to build the metal layers and passivation/openings), the UBM and C4 ordinary wafer bumping with solder are fabricated. Then, the structure is temporarily bonded to a carrier wafer. It is followed by backside back grinding, TSV fabrication and passivation/openings, and UBM.

Next is C2W face-to-back bonding, followed by debonding of the carrier wafer from the TSV wafer, and then the TSV wafer is diced into individual TSV modules. This TSV module is solder reflowed on a package substrate and test.

C.4) Wide I/O Memory (Face-to-Face) by TSV Via-Last (from the Backside) Fabrication Process: The FEOL, MOL, and BEOL processes are exactly the same as the (face-to-back) TSV via-last (from the backside) process. However, for the face-to-face case, after the UBM step, the device wafer is temporarily bonded to carrier #1 as shown in Figure 5. Then, the backside is subjected to back grinding, TSV fabrication, and passivation/openings from the backside of the device wafer. These processes are followed by UBM, C4 wafer bumping with solder, and temporary bonding to carrier #2; then debonding from carrier #1 is accomplished.

After the above processes are completed, C2W face-to-face bonding is done next. After C2W bonding, the carrier #2 wafer is debonded from the TSV wafer and diced into individual TSV modules. The TSV module is soldered on a package substrate, then test.

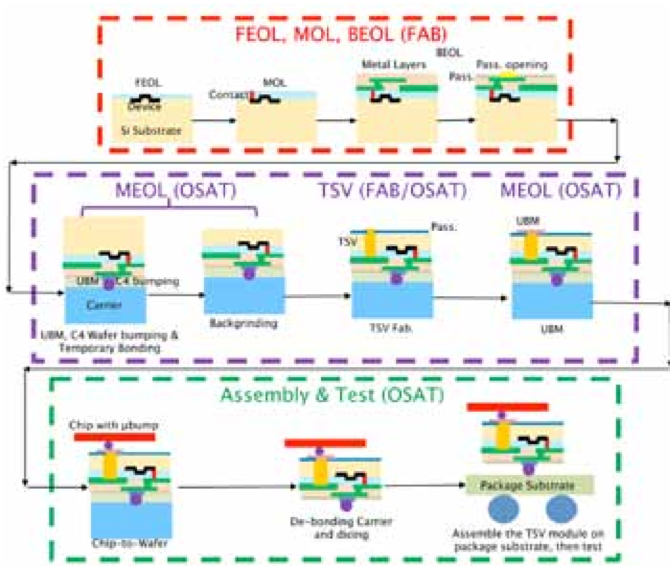

Figure 4: Critical steps and ownerships for (face-to-back) wide I/O memory using the TSV via-last from the backside fabrication process.

From Figures 4 and 5 it can be seen that the TSV can be fabricated by either the fab or OSAT. However, due to the logistics of the process flow, the chance for the fab to do it is very slim. (Once the wafer is out of the fab and processed by the OSAT, it is almost impossible for the wafer to go back to the fab

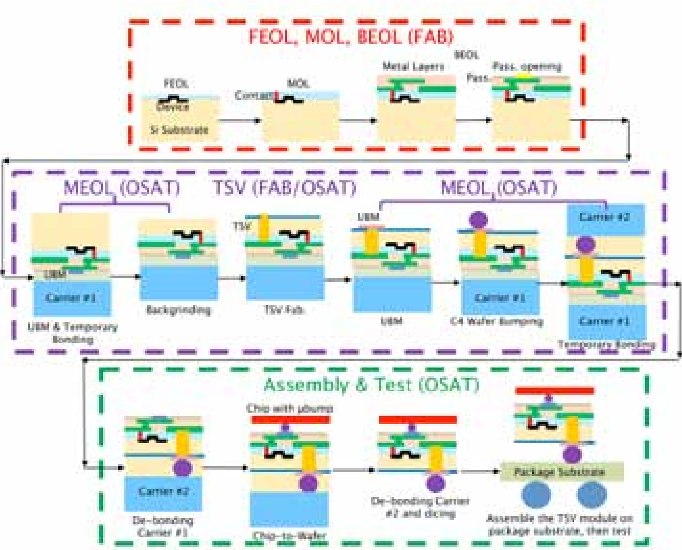

Figure 5: Critical steps and ownerships for (face-to-face) wide I/O memory using the TSV via-last from the backside fabrication process.

for further processing.) Also, because of technical issues, such as hitting the various embedded alignment targets in the x-, y- and z-directions (to enable the alignment between the metal layers on the topside of the wafer and the positioning of TSVs formed from the backside), it is very challenging for the OSAT. Thus, the TSV via-last (from the backside) fabrication process should be avoided until these issues are resolved.

C.5) Wide I/O DRAM by TSV Via-Middle Fabrication Process: After FEOL, MOL, TSV, and BEOL of the DRAM and SoC/logic wafers, the SoC/logic wafer will go through the same steps as shown in Figure 2 of section C.1 for face-to-back, or Figure 3 of section C.2 for face-to-face. For the DRAMs, UBM is done first followed by micro wafer bumping of the whole wafer. These processes are then followed by temporary bonding to a carrier wafer, back grinding, Cu revealing, and UBM. These in turn are followed by debonding of the carrier wafer and dicing of the TSV DRAM wafer into individual TSV DRAM chips as shown in Figure 6.

The next process is C2W (DRAM chip to SoC/Logic wafer) bonding (e.g., 2-stacking, 4-stacking, 6-stacking or 8-stacking). After C2W bonding, the carrier wafer is debonded from the SoC/Logic wafer and diced into individual hybrid memory cubes (DRAM-stacking + SoC/Logic). These steps are followed by assembly of the hybrid memory cube with over-mold on a package substrate, then testing.

C.6) Memory-Chip Stacking by TSV Via-Middle Fabrication Process: The critical steps and ownerships of memory-chip (either DRAM or NAND Flash) stacking are exactly the same as those of the DRAMs of the wide I/O DRAM case as shown in section C.5. However, instead of C2W bonding as in the wide I/O DRAM case, memory-chip stacking is accomplished by stacking the individual TSV chips first and then attaching them to a package substrate and over molded. Following these steps, the TSV memory-chip stacking module is attached to a printed circuit board such as the registered dual

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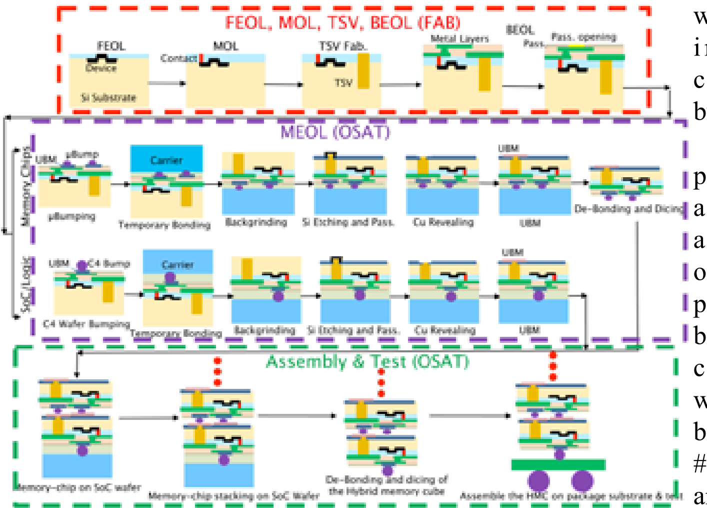
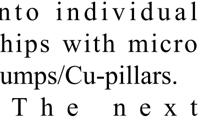


Figure 6: Critical steps and ownerships for wide I/O DRAM using the TSV via-middle fabrication process.

in-line memory modules (RDIMMs).

C.7) 2.5D IC Integration with TSV/RDL Passive Interposers: Figure 7 shows the critical steps and their ownerships. After the deposition of a passivation layer on a piece of dummy silicon (no active devices), the TSV can be fabricated, RDL can be built, and passivation/openings can be made. After the UBM, the TSV wafer is temporarily bonded to carrier #1. It is followed by back grinding, silicon etching, low-temperature passivation, and Cu revealing. Then, UBM, C4 wafer bumping with solder, and temporary bonding to carrier #2 are accomplished.

Separately, the device wafer without TSVs is subjected to either micro bumping with tiny solder bumps, or Cu-pillars with solder caps. The device wafer is then diced into individual chips with micro bumps/Cu-pillars.



The next processes to be accomplished are debonding of carrier #1, performing C2W bonding (the device chip to the TSV wafer). After C2W bonding, carrier #2 is debonded and the TSV wafer is diced into individual TSV modules. Finally, the TSV module can be assembled on a package substrate, then tested.

It can be seen from Figure 7 that the TSV and RDL can be made by either the fab or the OSAT. It depends on the layout, design, and fabrication capabilities, especially the line width and spacing of the RDLs. Usually, a few microns of line width and spacing can be done by the OSAT. Otherwise, it should be done by the fab.

Except vertically integrated companies, such as TSMC, who want to do the chip-on-wafer-on-substrate (CoWoS) process completely in house, most fabless design houses prefer the fab (e.g., UMC and GlobalFoundries) to make the blind TSVs and the RDLs of the passive interposer. Then, the fabs hand the unfinished "TSV interposer" off to an OSAT for MEOL (solder bumping/temporary bonding/thin wafer handling/back grinding/TSV revealing/debonding/cleaning), assembly and test. This is also true for the unfinished TSV device wafers.

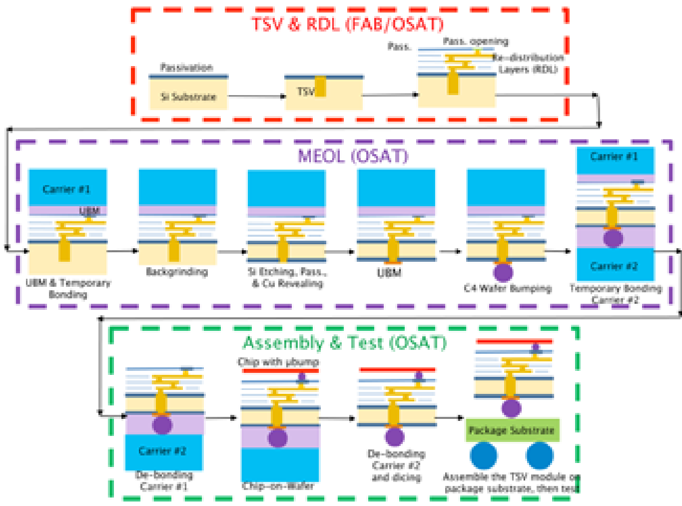


Figure 7: Critical steps and ownerships for 2.5D IC integration with a TSV/RDL passive interposer.

Summary

The technology supply chains for 3D IC integration manufacturing have been studied. Critical steps such as FEOL, MOL, BEOL, TSV, MEOL, assembly and test, and their ownerships for potential applications and HVM of 3D IC integrations such as memory-chip stacking, wide I/O memory (or logic-on-logic), wide I/O DRAM (or HMC), and wide I/O interface (or 2.5D IC integration), have also been provided and discussed. Some important results and recommendation are summarized as follows:

- For device wafers, TSVs fabricated by the via-last from the backside process should be avoided until the logistic and technical issues are resolved.
- For device wafers, TSVs fabricated by the via-middle process is the right way to go and should be performed by the fab.
- For passive interposers, TSVs can be done by either the fab or OSAT. For ≥3µm line width and spacing RDLs, either the fab or the OSAT can do it. Otherwise, it should be done by the fab.
- For both device wafers and interposer wafers, the MEOL, assembly and test processes should be done by the OSAT (except vertically integrated companies). It can be seen from Figures 2 to 7 that there are many important steps in the MEOL (solder bumping/temporary bonding/back grinding/TSV Cu revealing/thin wafer handling/debonding/cleaning), assembly and test; therefore, the OSATs should strive to make themselves ready for a robust and high-yield manufacturing process.
- In order to have a smooth hand-off from the fab to the OSAT of the unfinished TSV wafer, more research and development work should be performed on the testing methods for blind TSV wafers for electrical [20, 21], thermal, [22], and mechanical performance.

Acknowledgments

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(continued on Page 54)

Wafer-Level Test as Full Functional Test Increases Requirements for Spring Probes and Probe Cards

By James Brandes, Christopher Cuda [Multitest]

There are many differences between wafer probe and wafer-level test. Some are obvious and some are more subtle. There are both electrical and mechanical differences. These differences require that different contact technologies be used for wafer-level test than were used for wafer probe.

The original contact technique for wafer probe is cantilever-beam. It is inappropriate for wafer-level test because it is intended for peripheral bonding pads and is not readily adapted to either arrays of solder balls or multiple sites. More recent wafer probe technologies are vertical probe and membrane probe. Both of these are array-capable, but fall short in one or more categories of electrical or mechanical performance. These requirements dictate the use of spring probes for wafer-level test.

Wafer-level test considerations

Wafer-level test is final test, so the interface must have all the electrical capabilities traditionally associated with package test. The path must have low resistance for accurate DC measurements. High bandwidth is a requirement for at-speed functional tests or AC measurements. Bandwidth beyond the third harmonic means faster rise and fall times and crisper edges applied to the device and sensed by the tester. The entire path, but especially the contactor, should have low inductance for power delivery, to reduce the noise on the device under test's (DUT's) power and ground as its current requirements change at its switching frequency. The interface must also be able to conduct significant current both for power delivery and for some DC parametric tests. **Table 1** compares these parameters for various wafer-level contactor technologies. (Data was not available on the internet for all parameters for all technologies.)

There are several important mechanical considerations, such as force, tip geometry, probe length, and compliance. Unlike wafer probe, in which relatively clean aluminum or copper bond pads are contacted (typically in a clean room), wafer-level test makes contact to solder balls, often in a less-clean environment due to the additional processing involved with adding the redistribution layer and solder balls. Wafer-level test requires greater force to pierce thick tin oxides and (potentially) debris on the solder ball. Sharp probe tips are extremely important for piercing the solder ball to make contact to the clean tin inside without affecting solderability. While probe length is not an important parameter in and of itself, shorter probes will generally improve all the electrical parameters mentioned above.

The mechanical parameter on which this article is focused is compliance. (When characterizing probe cards, the term overdrive is used to describe the distance beyond initial contact that the wafer should be plunged into the contact set. For spring probes the term compliance is used to describe the total travel of the probe.) Probed wafers are extremely coplanar, and little compliance (overdrive) is required to make reliable contact to them.

Type Technology	CSP050 Pogo™ Probe	MER040 Spring Probe	MER030 [1] Spring Probe	Membrane	Vertical 1	Vertical 2
Inductance	1.22nH	0.9nH	1.7nH	0.2nH [2]	N/A	N/A
DC Current @ 20C	1.7A	1.8A	1.5A	200mA [3]	0.5A	1.6A
Contact Resistance	100mOhm typ.	70mOhm typ.	150mOhm typ.	< 200mOhm	< 2Ohm	N/A
Bandwidth	5.7GHz	18GHz	12.4GHz	20 - 33GHz	1.3GHz	N/A

[1]In Development [2]Tip Only [3]On Solder

Table 1: Key electrical properties of various wafer-level contact technologies.

Packaging considerations

Packaging, including wafer-level packaging, adds significant variation to the target height. This variation is expressed on the package outline drawing as the Z-height tolerance of the solder ball. Wafer-level test contacts must have more compliance than traditional wafer probe technologies to accommodate this tolerance. The greater the compliance of the contact set, the less effect underdriving the probe will have. Because of its external-spring design, Quad Tech probes have more compliance than traditional

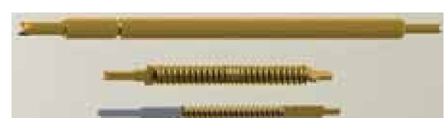

Figure 1: Pogo™-style probe (CSP050), and two Quad Tech probes: MER040 and MER030 (top to bottom).

probes. **Figure 1** shows the relative sizes of a Pogo probe and two Quad Tech probes. These probes are suitable for pitches of 0.5mm, 0.4mm, and 0.3mm, respectively.

The first probe with an external spring was the Bantam®, introduced about thirteen years ago; the architecture provided improved force and compliance in a significantly shorter probe. The Quad Tech probe retains the advantages of the external spring design, is more cost-effective to manufacture, and is scalable to the finer pitches required for wafer-level test. **Table 2** shows several key mechanical properties among various probe technologies that are used for wafer-level test. The compliance of the membrane probe is a bit misleading. The contact points are not individually compliant. In fact, if adjacent contact points vary by more than 0.05mm (as when there is a missing solder ball) the contact set can be damaged at touchdown.

In addition to the contactor, the probe head includes a printed circuit board (PCB). PCB planarity is also important. Spring probes make solderless contact to the PCB, and these probes are preloaded on the PCB side of the contact set to prevent pad-damaging chatter with each touchdown. Any deviation from planar consumes some of the spring probe compliance. As wafer-level contactors grow larger and test parallelism increases, the distance between the probes, which are furthest apart, grows. As the distance grows, planarity becomes more difficult to achieve. The distance between the two furthest probes is growing as higher pin count devices are tested at the wafer level, and various test site patterns are employed to leverage the economic advantages of wafer-level packaging and test.

Controlling PCB planarity starts with the PCB's layer stack-up in the design. Using evenly-distributed planes through the layer stack and adding non-functional copper pour (known as thieving) are common practices employed to maintain planarity. As test speeds have increased, we have conducted extensive tests to ensure that the copper pour is executed in a way that ensures it will have no negative effect on electrical signal performance. **Figure 2** shows an inner layer from an ATE board where floating thieving has been added to the blank areas of a signal layer to more evenly distribute copper across the surface.

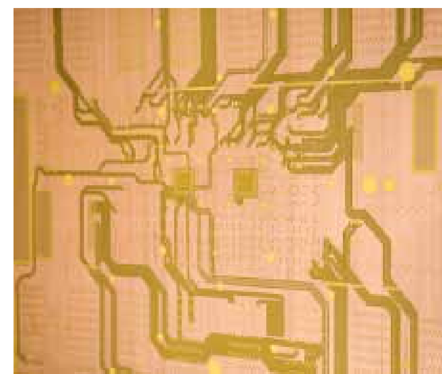

Figure 2*:* Copper thieving on a PCB signal layer.

Figure 3 shows an example of a balanced, mixed-dielectric stack up where the Rogers® brand material is used for the high speed signals, and the Nelco® brand material is used for the balance. The key attribute is that the thicknesses of each are chosen to maintain symmetry from the center. As each material will move differently during lamination, keeping the symmetrical balance minimizes the material-mismatch impacts on the overall warp of the PCB.

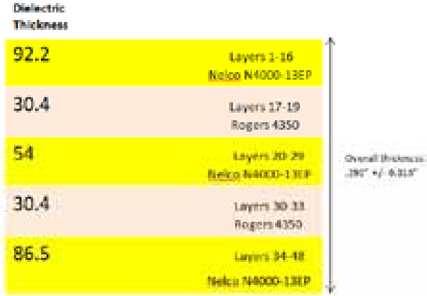

Figure 3*:* Balanced, mixed-dielectric layer stack-up.

When mixed laminate materials are required for signal integrity purposes, careful consideration must be made to ensure a proper match of the laminates' resins, especially their coefficient of thermal expansion and weave direction. A mismatch will cause excessive warp or delamination, robbing the contactor probes of their valuable compliance and affecting the parallelism of the contact set and the target wafer.

Wafer-level package testing applications commonly require 0.4mm ball pitch. At this pitch, and with the thicknesses required for rigidity and routing layers, most PCB manufacturers require multiple lamination cycles. However, there is a planarity benefit to manufacturing with monolithic books (one lamination cycle). To accomplish a monolithic build, the PCB requires high-aspect ratio vias. Less stress occurs on the laminate resins of PCBs built with a single lamination cycle. The undesirable stress contributes to PCB warp. The examples in **Figure 4** show two different build methods for a 0.4mm pitch, 49 pin, 7 x 7 ball array. The pad array density necessitates four signal layers to escape the DUT area. **Figure 4a** shows a multiple lamination approach, and **Figure 4b** shows a single lamination. In the multiple lamination approach, micro vias and blind vias are used to escape the DUT pattern; the multiple laminations keep aspect ratios low for easier plating. Single lamination requires the use of smaller vias, higher aspect ratios, and smaller antipads.

Regardless of the number of

Type Technology	CSP050 Pogo™ Probe	MER040 Spring Probe	MER030 [1] Spring Probe	Membrane	Vertical 1	Vertical 2
Test Height	6.45mm	3.3mm	3.5mm	0.065mm [2]	3 - 7mm	5.95mm
Compliance	0.51mm	0.44mm	0.55mm	0.25mm	0.125mm	0.3mm
Min. Array Pitch	0.5mm	0.4mm	0.3mm	0.15mm	0.15mm	0.2mm
Force @ Test Height	35g	30g	25g	16g	25g	6g @ 0.2mm
Tip Shape	3 or 4 points	two points	two points	one point	one point	four points
Probe Mark(s)	off apex	off apex	off apex	at apex	at apex	off apex

[1]In Development [2]Tip Only

Table 2*:* Key mechanical properties of various wafer-level contact technologies.

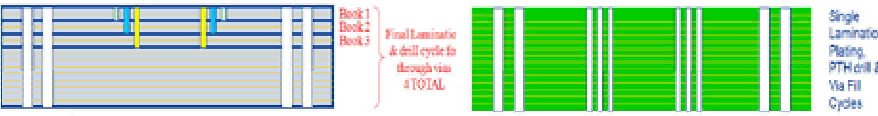

Figure 4: Comparison of a) multiple lamination and b) single lamination.

lamination cycles, there is always some element of bow and twist in a PCB as well as the football effect. The term football effect was coined to describe the shape the PCB panel can take on after lamination: The PCB panel resembles the shape of an American football, where the center of the panel is thicker than the outer edges (**Figure 5**). We have developed a process for eliminating the football effect, called UltraFlat™. This new process improves planarity by subjecting the panel to a series of polishing steps to eliminate the height differences across the panel. The process also provides permanent improvement to the planarity of the PCB. Other traditional processes of improving PCB planarity such as flat-baking only offer a temporary improvement. As flat-baked PCBs age and take on moisture from atmospheric humidity, the PCBs will return to their pre-baked shape.

Figure 5: Comparison of an UltraFlat Board with a typical football-effect board.

Validation of planarity is a challenge in itself. In recent years, users have tightened warpage tolerances in hopes of capturing planarity. Final test ATE boards for many years have used 0.5% as the pass limit for PCB warp (>0.005"of warp per inch of diameter of the PCB causes the PCB to be rejected). The most common method of measuring PCB warp employs a pin gauge around the perimeter of the finished PCB atop a flat granite surface. This method is simple, but does not provide the information that is most important for wafer-level testing because it measures overall PCB warp, instead of planarity in the DUT area, which is typically in the center of the PCB. A test interface can allow considerably more warp on the outer edges of the PCB, whereas the center/DUT pattern planarity is most important, both because of the limited contactor probe compliance and the requirement to maintain parallelism to the target wafer. Therefore, planarity in the contactor area must be held to a much tighter tolerance. We recommend a maximum warpage tolerance of 0.3% for spring probe contacts in wafer-level test applications. Whenever possible,

Figure 6: ATE board flatness measuring technique.

a DUT tolerance of 0.15% should be used for optimum performance of the interface.

Summary

As PCB planarity and warp tolerances are reduced to meet the needs of future wafer-level testing, the industry needs changes in PCB planarity validation techniques. Current methods vary from the standards put forth by the IPC to customized methods that confirm the planarity where it matters for a particular contact technology. In this paper, we suggest a method for wafer probe and wafer-level test that uses a height gauge as a true measurement of DUT-area planarity. The height gauge is zeroed on one plated pad location in or next to the critical DUT area, and then measures the height at predetermined pads around the critical areas as defined by the user. The delta between all the points is used to determine a pass/fail criteria using a system of allowable units of deviation. This output can be expressed as a percentage, or as a maximum value of the delta. Because of the inconsistencies in common laminates, measuring a plated surface offers a more consistent and application-relevant surface height versus measuring the laminate surface. Because of the mechanical contact required for this method, we recommend users include depth gauge test pads in the design that are not electrically connected to the rest of the PCB so that pogo landing pads are not touched. To eliminate the underlying surface variability, a flat granite block should be used as the base; then, to eliminate the bow and twist of the non-critical areas of PCB, use three identical posts at equal distances apart to hold the PCB above the surface of the granite block (**Figure 6**).

The unique challenges of wafer-level test require a fresh look at the mechanical requirements of the interface. Traditional probe technologies and PCB construction methods can have a negative impact on yields or test hardware life, which adds to cost of test in production.

Acknowledgments

Pogo is a trademark, and Bantam is a registered trademark of Everett Charles Technologies. Rogers is a registered trademark of the Rogers Corporation.

Nelco is a registered trademark of the Nelco Corporation. UltraFlat is a trademark of Multitest.

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Package-Level Circuit Modifications Using Plasma-FIB to Create Functional Prototypes

By Peter Carleson, Brian Routh Jr., Trevan Landin, Kenny Mani [FEI Company]

Plasma-based focused ion beam (PFIB) systems have now been used successfully to create prototypes that incorporate package-level modifications. Packaging plays an increasingly important role in improving the performance of integrated circuits [1]. Multichip packages allow the integration of different types of ICs to provide better performance and greater functionality in less space. This is particularly true of circuits intended for mobile applications where space is limited by the handheld nature of the device, and digital, analog and radio frequency components must be tightly integrated. Equally important, signal routing for analog and RF circuits can have significant performance effects that are difficult to model and may not become apparent until the circuit is packaged and tested [2,3]. Making design changes and creating new prototypes can take 1-2 weeks for package-level modifications, whereas it takes 6-8 weeks for die-level changes that require new masks and new silicon. The PFIB technology can make modifications in less than a day, significantly shortening the design and test cycle.

FIB circuit modification has been used for many years at the die level where it allows manufacturers to implement and test changes without repeating the lengthy process of creating new masks and fabricating new silicon. Die-level circuit elements typically have dimensions of a few micrometers or less. Modifications to features of this size can be accomplished in a matter of hours with conventional FIB systems that use liquid metal ion sources (LMIS). Circuit elements at the package level are much larger and the time required to modify them with conventional FIB is prohibitively long. In some cases, the features are large enough (>100µm) to permit modifications with laser-based systems [4], however, advanced packaging processes now coming into production frequently use signal traces in the middle range (10µm - 100µm), too big for conventional FIB modification and too small for lasers. PFIB, which uses a plasma source rather than LMIS, can generate higher current ion beams with milling rates 20 to 100 times faster, permitting modifications of these advanced package circuit elements within a practical time frame [5-8].

System Configuration

The Vion PFIB used in the work described here is configured similarly to conventional FIB systems. The primary differences are the inductively-coupled plasma source and a three lens column specially designed to deliver beam currents ranging from 1.5pA to more than 1µA. It includes a 150mm piezo-ceramic stage, a detector for secondary electron and secondary ion imaging, a gas injector system (GIS) for gas assisted etching and deposition, an electron flood gun for charge neutralization, both optical and infrared (IR) microscopes, CAD (computer aided design) overlay and navigation software, job automation software, and access to specially adapted applications protocols and methods.

Comparing Liquid Metal and Plasma Sources

In the LMIS used in conventional FIB, a liquid metal (gallium) flows from a reservoir along the surface of a sharply pointed electrode. At the very fine tip of the electrode a strong electric field ionizes metal atoms and accelerates the ions toward the sample into the focusing column. In a plasma source, a gas (typically xenon, though other gases may be used) flows into a cell surrounded by a helical antenna. The antenna couples energy into the cell, ionizing gas atoms to create a plasma. Gas ions exit the cell through a small aperture into the extraction optics where a strong electric field accelerates them into the focusing column. The LMIS can be considered a point source with low angular intensity (0.02mA/sr). The plasma source is broader in extent but offers a high angular intensity (50mA/sr). Because the LMIS is so small (50nm diameter), it requires little or no demagnification to form a small diameter beam, however, space charge effects cause strong spherical aberrations that dramatically expand beam diameter at high beam currents. The plasma source (which may be 15µm in diameter) requires strong demagnification to achieve small beam diameters, but can maintain smaller beam diameters at high currents. Below 10nA, LMIS beams may have diameters as much as an order of magnitude smaller than plasma FIB. The cross over in performance occurs at 50-60nA. Above this value, the LMIS beam diameter deteriorates rapidly and plasma sources can deliver more current into smaller beams. The Vion PFIB provides spatial resolution of <25nm at 1.5pA and 2.3µm at 1.3µA.

The Xe+ ions created by the plasma source have nearly twice the mass of the Ga+ ions from a liquid metal source. On some materials they provide higher

sputtering rates (the average amount of material removed by each ion). The increase is material dependent and ranges from 1.0 to 1.6 times higher for materials commonly used in integrated circuits, with significant increases for Si, Al and Cu. The combination of 1X to 1.6X higher sputtering rates with 20X to 60X increases in beam current results in overall material removal rates 20X to 100X faster. The PFIB offers clear advantages for applications where fast material removal is the first priority, such as package-level circuit modifications, while still preserving solid performance at lower currents. The increased material removal rates reduce total processing time for package-level circuit modifications from days to hours, making PFIB a practical tool for this application.

Navigation

Simply finding the circuit elements to be modified can be challenging for a packaged circuit. Removing the package, a viable option for failure analysis, is not an option when trying to create a modified but functional prototype. Depending on the application, it may also be necessary to locate the circuit elements through the "flipped" silicon substrate. An optical microscope (NavCam) mounted on the sample chamber door assists with initial navigation by providing an optical image registered with the coordinate system of the FIB when mounting the sample on the stage. The operator can use the NavCam image to navigate directly to the location of interest based on external package features such as solder balls. Navigation software is available to overlay CAD data on the image, from package level signal pathways down to circuit elements within the die. When needed, an infrared microscope provides imaging capability from the backside of the die through the silicon substrate. Finally, imaging with the scanning ion beam, using either secondary electrons or secondary ions, provides high resolution and strong contrast.

Gas-assisted Milling and Deposition

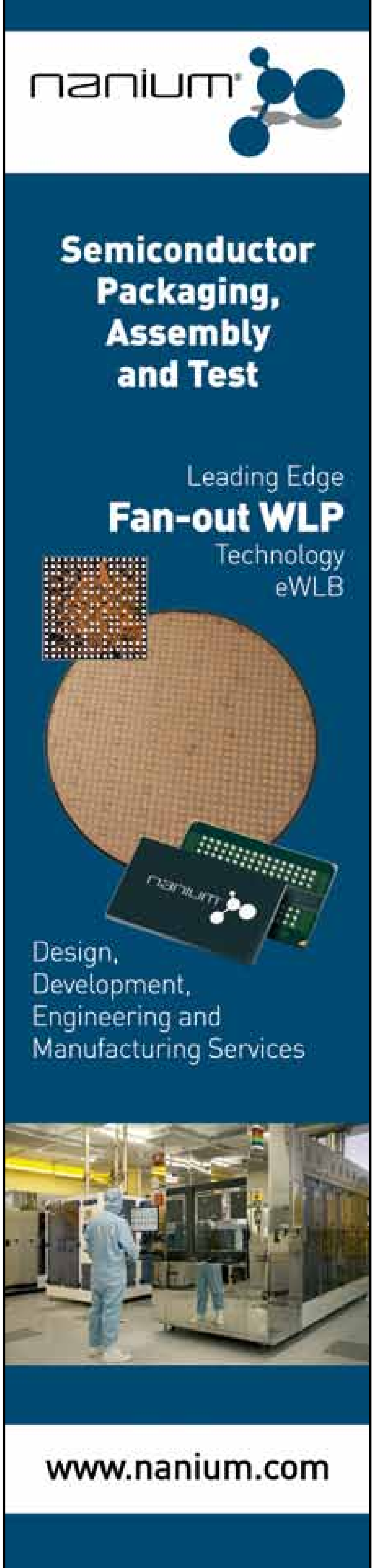
Although the ion beam alone will mill most materials, milling speed can be increased by introducing small amounts of specific gases through an injector needle at the milling site. Because different gases increase milling rates differentially for specific types of materials, this selectivity can be used to restrict milling to certain features, or to stop milling when a particular interface is reached.

Xenon difluoride (XeF_2) is used in conventional FIB to enhance milling rates on silicon, especially when removing large volumes of the silicon substrate to access circuitry from the backside of the die. In the PFIB, XeF_2-assisted etching generates flat floored trenches even at 1.3µA beam currents. Volume removal rates typically range from 400k to 600k-μm^3/min, 3 to 4 times faster than Ga FIB. Nwell contrast appears in the FIB image 2 to 4µm before the etch surface reaches the circuitry, providing an effective endpoint for the etch process.

A metal organic precursor gas (in this case, methlycyclopentadienyltrimethyl platinum) can be used to deposit metal lines. When the gas molecules are decomposed by the ion beam, the metal deposits on the surface and the volatile organic components are pumped away by the vacuum system. Xe exhibits higher Pt deposition efficiency (average volume deposited per ion) than Ga. Although the Pt deposited by PFIB exhibits higher resistivity than Ga FIB, this can be compensated by depositing thicker lines to lower total resistance.

Similarly, insulators can be deposited by using a precursor gas, such as hexamethylcyclohexasiloxane HMCHS). Preliminary results indicate that oxide depositions performed with Xe are significantly more resistive than depositions performed with Ga. Resistivities appear to be >>10^{16} µΩ•cm.

A special O_2-assisted process has been developed to etch polyimide using low beam energies to avoid damage. Highly textured surfaces can form during PI removal, but the high selectivity of the gas-assisted removal allows the



underlying metal or oxide to serve as an effective etch stop.

Charge Neutralization

Charge can accumulate rapidly when milling insulating materials with positive ions, ultimately interfering with milling and imaging processes. A defocused electron flood gun directed at the milling site supplies electrons to neutralize charge buildup.

Application examples. Figures 1 through 6 illustrate application examples of package-level device editing.

Figure 1 shows a sample that has been tilted to show the cut more clearly. The access window is several hundred microns in length. The process took 30 minutes to pump down, align, and cut with the Xe beam, and another 3 minutes for XeF_2 cleanup. The opening was subsequently filled with a 5 minute insulator deposition so that when the solder is re-flowed it does not flow into the cut box.

Figure 2a shows CAD data that has been overlaid on the FIB image to locate a buried signal line and an access window has exposed the line. **Figure 2b** is a close up of the access window in which the copper line is visible crossing diagonally at the upper right corner. **Figure 2c** shows that the line has been cut and the copper completely removed leaving the underlying fiberglass filaments and epoxy substrate visible at the bottom of the hole.

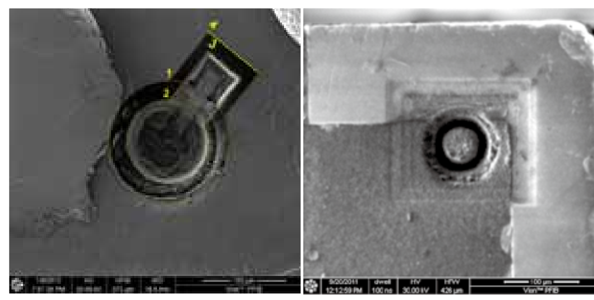


Figure 3: a) Two circular (1 and 2) and two rectangular patterns (3 and 4) are combined to create exclusion zones; and b) An example of via isolation from copper pad using a donut-shaped dual concentric circle pattern.

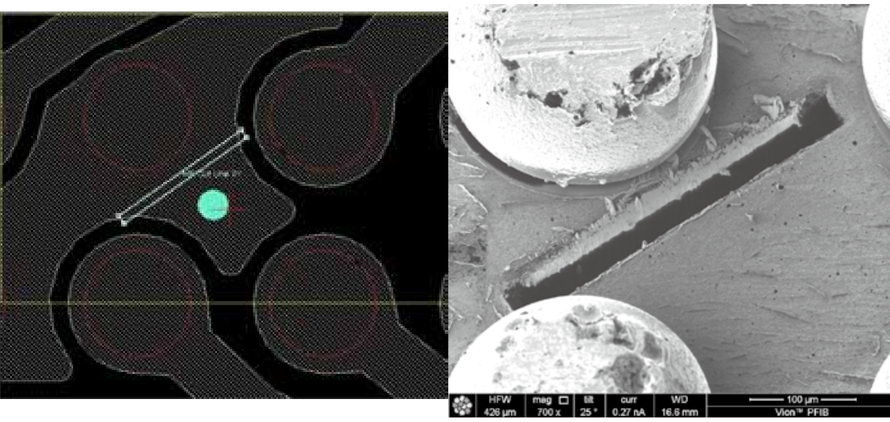


Figure 1: a) (left) The redistribution layer is visualized with CAD overlay and the cut is defined; and b) (right) An FIB image showing the access window milled through the overlaying solder mask and the cut RDL below.

Sometimes complex etch and deposition patterns are needed as shown in **Figure 3**. On the left, two circular (1 and 2) and two rectangular patterns (3 and 4) are combined to create exclusion zones to protect deposited platinum from cleanup while preventing shorting to other components. On the right is an example of via isolation from the copper pad using a donut-shaped dual concentric circle pattern that enables visual verification of the complete separation between the pad and the via. This is the simplest method of disabling a via/pad connection. PFIB provides better accuracy than previously obtained using a laser. The outer diameter is 75μm, the inner diameter is 50μm. The process took less than 5 minutes at a beam current of 0.57μA.

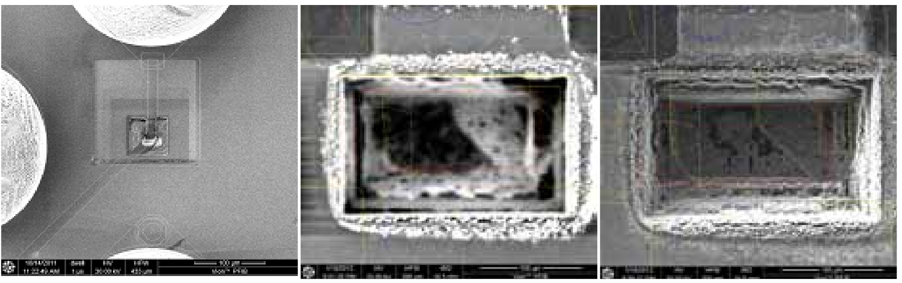


Figure 2: a) (left) CAD data has been overlaid on the FIB image; b) A close up of the access window; and c) The line has been cut and the copper completely removed.

Plasma FIB modifications are not limited to substrate alone and can be executed directly on the circuitry of wafer-scale packages. The inherent challenges of FIB milling through polyimide can be overcome with optimized choices of current, accelerating voltage and gas, enabling modification directly onto the die. **Figure 4a** shows the Pt jumper, several hundred microns long, deposited directly on top of the polyimide. **Figure 4b** is a close up near the left end of the jumper showing the cut buried signal line. **Figure 4c** is a close up of the connection at the right end of the jumper.

In this modification shown in **Figure 5**, a probe was used to temporarily move gold bond wires, providing access to copper traces below, which needed to be swapped at the bond fingers. The image shows the nudged wires and the initial beam-deposited platinum connection. The gas injector nozzle is visible in the upper right corner of the image.

Figure 6 shows a complex signal swap with the cutting of adjacent traces and re-routing of signals using deposited metal lines and insulation. A final coating of insulation will prevent corrosion and shorting.

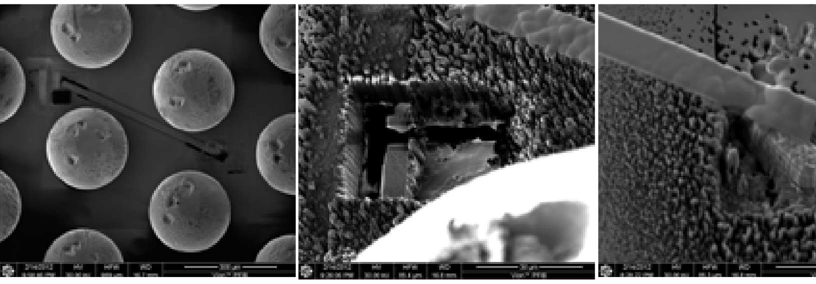


Figure 4: a) (left) A Pt jumper, several hundred microns long, deposited directly on top of the polyimide; b) (middle) Close up near the left end of the jumper showing the cut buried signal line; and c) A close up of the connection at the right end of the jumper.

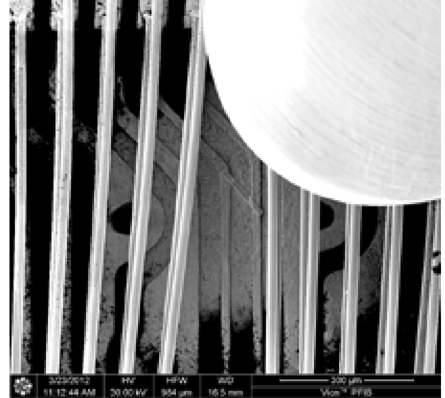


Figure 5: Copper traces below gold bond wires that were swapped at the bond fingers. The image shows the nudged wires and the initial beam-deposited platinum connection.

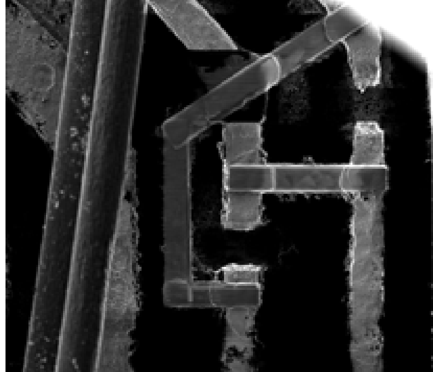


Figure 6: A complex signal swapped with the cutting of adjacent traces and re-routing of signals using deposited metal lines and insulation.

Summary

Many RF and analog circuits are strongly influenced by the interconnect routing layers in the package. Electrical effects, such as inductance and ground loops, can be difficult to model and simulate precisely, thereby requiring multiple design changes to confirm theories and fixes before production volumes can ramp. Plasma FIB technology has been a key to enabling rapid prototypes with layout changes in the package to improve the electrical performance of the existing product. These samples can be created and tested in one day to allow rapid design and layout changes to be verified.

Substrate modifications in general, and plasma FIB operations in particular, have improved our ability to make design modifications and create future design possibilities. This method lends itself well for those tasks that are too small for laser and too big for traditional FIB tools. As we have progressed in our methodology, we have applied the process to substrate modifications, wafer-scale package modifications, IC FIB modification, TSV cross sections, solder ball cross sections, MEMS cross sections, backside FIB trenching, gallium-free metal depositions, and artifact-free failure analysis cross sections that accurately preserve the failed condition.

Acknowledgments

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Functional Testing of 0.3mm-pitch Wafer-Level Packages to Multi-GHz Speed

By Ila Pal [Ironwood Electronics]

Today's electronic packages have high clock speeds (in the multi-GHz range), fine pin densities (below 0.4mm pitch) and high pin counts (over 1000). When these packages are assembled onto a printed circuit board (PCB), they perform certain functions at a certain speed. Socketing is one of the avenues to test the functionality of IC packages without damaging them. Socketing these high-speed and high-density IC packages requires an innovative solution to the challenges of designing a shorter signal path (less resistance), good electrical insulation (prevents signal loss), and proper thermal management. Design of the socket is dictated not only by the functions mentioned above, but also by other parameters such as durability, power consumption, assembly methods, and the environment in which the system will operate. The Silver Ball Matrix (SM) GHz socket (**Figure 1**) provides a solution that is fast, dense and durable.

Figure 1*:* Silver Ball Matrix (SM) GHz socket.

Socket Function

A socket can be defined as an electromechanical device that provides a removable interface between the IC package and system circuit board with minimal effect on signal integrity. Having a removable interface is the major reason for using a socket and it is required for a variety of reasons, including ease of assembly, reworking, upgrading and cost savings. The cost advantage is saving the IC by not attaching it permanently to the PCB. The socket is semi-permanently (solder-less) attached to the PCB, while the IC device can be inserted into or removed from the socket without disturbing the connections to the PCB. A socket helps to test, evaluate and inspect the complete system. Sockets also allow for maintenance, testing, and replacement or upgrades in the field. This in the field capability becomes a critical factor because of the pace of technology evolution.

A GHz Socket Solution

We have developed a sequel to the standard GHz socket that can test IC packages with a 0.3mm pitch. The SM GHz Socket provides a range of high-speed, high-density socket solutions from very compact production sockets to robust test and prototype applications. A cross section photograph revealing SM contacts is shown in **Figure 2**. The sockets are designed such that force is evenly distributed on the top of the IC, pushing the solder balls into very high speed, Z-axis, silver ball columns. The new contact has precise silver balls held together by a proprietary conductive formulation. These conductive columns (diameter optimized for 50 ohm impedance) are suspended in a nonconductive flexible elastomer substrate with a patented solid core for enhanced durability and reliable performance over time, temperature and cycles. This flexible substrate is compliant and resilient and enables the conductive columns to revert back to their original shape when the force is removed. Elastomer is the only medium between the IC package and the circuit board. A heat sink screw and the socket body provide heat dissipation for the IC in the socket. Precision guides for the IC body and solder balls position the device for connection.

Figure 2*:* Cross section of SM contacts.

Mechanical Characterization

Removable interface requirements are generally stated in terms of the insertion/extraction force and number of insertion/extraction cycles a socket can support without degradation. Insertion/extraction forces become increasingly important as the pin count of the device increases. Additionally, as the ICs are direct silicon (wafer), they are very delicate as opposed to enclosed packages, so the insertion force is also an important consideration. The first test examines the relationship between deflection of the contact, force and the contact resistance. A displacement force (DF) test station was used to measure the contact deflection and its corresponding force. Force increases linearly as the displacement increases. Similarly, the contact resistance decreases as the force increases. A stable contact resistance has to be identified based on the minimum force required. A desired displacement has to be identified based on the compliance

requirement of each device/application. This information is very important for the test engineer to set up failure criteria when performing the device test using this contact technology.

The second test examines the relationship between contact resistance over contact life cycle count. An actual handler was used for this experiment. A contact set consisting of 44 leads and 16 ground leads (QFN configuration) was mounted on the test board, which was then connected to a tester. A gold-plated shorted device simulator was mounted on the plunger head. The test set up was adjusted such that the head moved down 0.3mm, which was the chosen travel for the SM contact. Initial contact resistance data was measured via the tester and the automatic test equipment (ATE) was turned "on." This moves the plunger back and forth, which in turn cycles the SM contact. A digital counter was inserted into the test setup to measure the cycle count. The test setup includes a cycle speed of ~2,500 actuations/hour, a dwell time of ~0.7s, and is conducted at ambient temperature. The test vehicle was designed for a 7x7mm 44 lead, 0.5mm QFN shorted device simulator. No cleaning was performed to the gold-plated device under test (DUT) or to the SM contact. Contact resistance data collected at different cycle intervals is shown in Figure 3.

It can be seen from the graph that the average contact resistance is less than 25m-Ohms over 1,000,000 cycles. The standard deviation was also shown to provide an understanding of the data spread. Based on the graph, it can be concluded that the contact operates over 1,000,000 cycles with 25m-Ohms average contact resistance. The experiment was repeated with different lots manufactured at different times. The data is consistent over the different lots except the average is shifted down by 5m-Ohms. This shows that the process variations can cause a shift in contact resistance within 5m-Ohms. Similarly, the contact was tested at various temperatures and the acceptable range was defined as -50C to +150C.

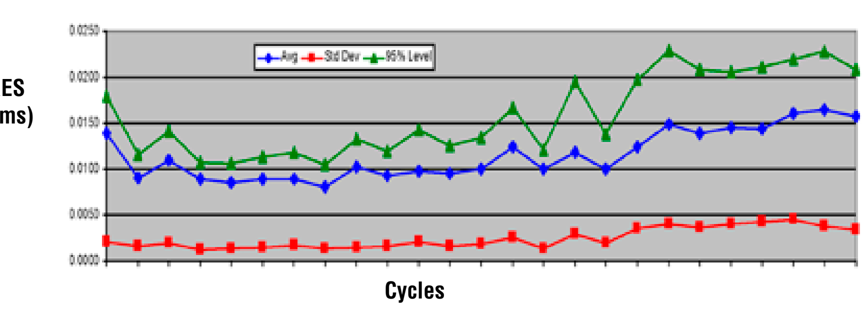


Figure 3: Contact resistance data collected at different cycle intervals.

Electrical Characterization

Electrical requirements are generally stated in terms of the bandwidth and current carrying capacity. Current capacity is determined by injecting drive current in steps of 10mA to a maximum value of 5A. For temperature as a function of resistance, dwell time is set to 3 minutes per data point to allow temperatures to stabilize. Results are shown in Figure 4. From the graph, it can be seen that for a 4A continuous current, the temperature rise is 14C. It is important for the test engineer to know that there is no joule heating effect due to the contact's base structure.

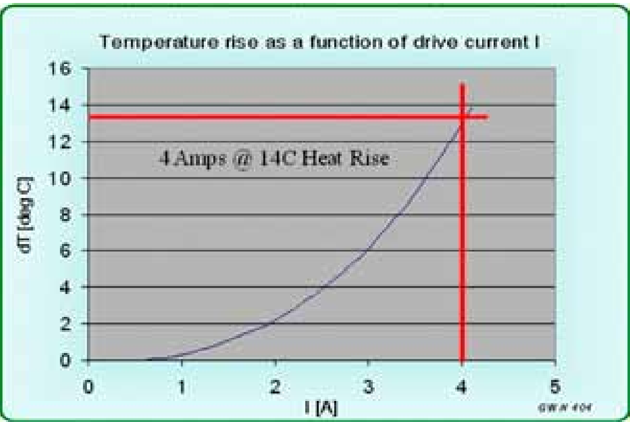
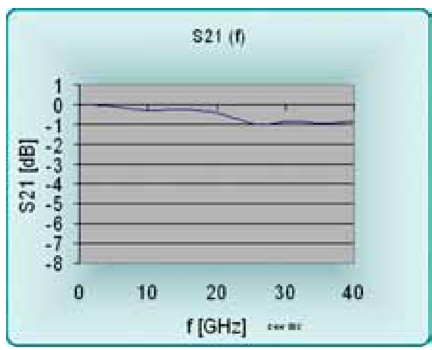


Figure 4: Temperature as a function of drive current

Measuring the bandwidth at final test determines if this contact technology is right for a particular test application. Bandwidth is typically specified in terms of insertion and return loss. A vector network analyzer is used for this experiment. A signal is sent from port 1 (top of the contact) and received at port 2 (bottom of the contact). Signal reflections are measured and reported as S21 curves (Figure 5).

An insertion loss of -1dB @ 40GHz is interpreted as 90% of the signal pass through the interconnect medium and only 10% of the signal is lost through the interconnect transition at 40GHz. It is important to note that the IC functionality is being verified at a specific frequency.



Insertion Loss - 1dB @ 40GHz

Figure 5: Signal reflections measured and reported as S21 curves.

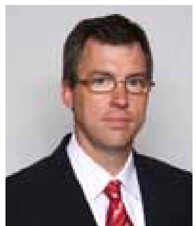
Summary

A primary concern to anyone utilizing high-density WLPs is that the socket must provide a high performance, low and stable value of resistance while meeting mating requirements. In particular, the mating force and the number of mating cycles the socket can withstand without degradation are key. SM GHz sockets address these concerns.

Biography

Ila Pal received his MSME from Iowa State U. and an MBA from St. Thomas U. He is VP of Marketing at Ironwood Electronics; email ila@ironwoodelectronics.com

Deca Technologies: Growing Up in Tough Times



After a year of being in virtual stealth mode, interconnect start-up Deca Technologies recently launched its second product family, the M-Series, an embedded die packaging technology featuring its proprietary Adaptive Patterning software technology. Chip Scale Review talked to Chris Scanlan, VP of product management, about the company's first full year in business, recent accomplishments, and future plans for the company.

CSR: The company was launched during one of the worst worldwide economic crises. What has it been like to become a player in the advanced packaging sector and to ramp production under these conditions?

CS: We have been very fortunate to have customers respond favorably to our value proposition, which is based on a fundamentally different way to manufacture wafer-level interconnect. Our focus has been to achieve our development milestones on schedule, and to complete qualifications and initial production ramp for our launching customers. As a start-up, our success thus far has been largely a function of our ability to execute. We have been less affected by macroeconomic cycles.

CSR: Market analysts have predicted that 2013 will be the beginning of an upturn in the industry, driven by the demand for mobile and wireless devices. Many technology advances are expected to address the performance, power and form factor needs of these devices. How is Deca positioned to address this demand?

CS: Our launching product line is a fan-in wafer-level chip-scale package (WLCSP), as well as the requisite test and die finishing services. WLCSP is one of the fastest growing semiconductor package types, particularly in mobile and wireless applications. We are able to take advantage of this trend with a differentiated service offering focused on speed, flexibility, and lower cost-of-ownership (CoO). Our factory was designed from the ground up with the flexibility to run 200mm or 300mm wafers without change-over, so we have the capability to respond quickly to changing demand without dedicated capital investment. Our new M-Series fully molded CSP is positioned to offer the electrical and thermal benefits of flip-chip CSP with the smallest possible form factor and a cost that is competitive with wire bond BGAs. We're already seeing strong interest in the technology, particularly for mobile and wireless applications.

CSR: The M-Series has been compared to fan-out wafer-level packages (FOWLP) like the embedded wafer-level ball grid array (eWLB), yet it is structurally different than eWLB. What are the main distinctions between the M-Series and FOWLP? What are the target applications for the M-Series?

CS: M-Series is a fully encapsulated, rugged package structure that has the look and feel of a molded flip-chip CSP package (Figure 1). Both the structure and the manufacturing process have been designed to avoid the chronic issues with typical FOWLP technologies. The balanced structure allows us to avoid excessive panel warpage and eliminate non-value added steps typically required to maintain panel flatness. The die is fully protected by epoxy, and the panel level redistribution is performed on a flat surface with no die-to-mold compound transition. This simplifies the copper redistribution layer (Cu RDL) patterning process and allows us to apply advanced design rules to the entire unit (Figure 2). The panel format has been co-designed with our WLCSP manufacturing infrastructure to allow M-Series panels to run through our process interchangeably with Si wafers. This increases capital efficiency and avoids costly conversions. We have also developed a proprietary patterning

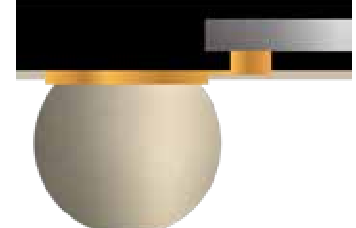


Figure 1: M-Series fully molded device structure.

Figure 2: Cross section view of the M-Series.

technology that finally resolves the die-shift problem, resulting in both higher interconnect yield and higher die-attach throughput.

M-Series is ideal for devices requiring the smallest possible form factor (x,y, and z) that are unable to utilize conventional fan-in WLCSP. Its electrical performance and miniature outline offer an attractive alternative to flip-chip and wire bond BGAs, CSPs in smartphones, or other high-density applications.

CSR: In your paper at IWLPC, you described the Adaptive Patterning™ process. Can you briefly summarize how that works? Can it be applied to packages other than the M-Series?

CS: Adaptive Patterning is actually a suite of design and manufacturing technologies that resolves the die-shift problem that has plagued embedded die technologies for two decades. The process of embedding an array of die in a substrate panel or molded wafer results in some variability or shift of the die with respect to the target position. When you then try to align a routing pattern to the entire panel, or to a portion of the panel, the interconnect pads on the die don't perfectly align to their respective vias and capture pads in the build-up routing layers. This can result in yield loss. Typical solutions to the die-shift problem include using high-accuracy, slow speed die-attach machines and modifying chip designs to increase the size of the die bond pads.

The adaptive patterning process works by dynamically adjusting a portion of the RDL pattern to accurately connect to the bond pads or other structures on each individual die in the embedded die panel. After placing an array of chips on a panel using a high speed placement machine, the actual position and rotation of every die on the panel is measured. This data is ported to a proprietary design tool that adjusts the fan-out unit design for each package on the panel so that the via layers or RDL patterns are properly aligned to bond pad features on the die. The individual package designs are then combined to form a drawing of the full panel for each of the layers that need to be adjusted, typically including the first via layer on the panel and the first RDL layer. The designs for each panel are transferred to a lithography tool, which uses the design data to dynamically apply a custom, adaptive pattern to each panel. The under bump metallurgy (UBM) pads are held constant to maintain conformance to the package outline specifications. Adaptive Patterning allows us to target smaller bond pads associated with advanced Si nodes with higher yield while using lower cost, faster die placement equipment. It also allows us to design M-Series around die that are designed for wire bond or flip-chip interconnect without imposing special constraints on the chip design.

This technique could be applied to any embedded die process wherein die are placed in a fixed position before forming an interconnect pattern over the die. This would include embedded chip in substrate and FOWLP, among others.

CSR: What's next on the drawing board?

CS: Deca's approach is to identify seemingly insurmountable problems that are holding back the industry, and then to challenge all core assumptions en route to a solution. Our first product offering, a fan-in WLCSP, is structurally similar to industry standard WLCSP offerings. Under the hood, we have completely rethought the wafer-level interconnect manufacturing process. We drew inspiration from SunPower Corp. to create a flow-line approach to wafer-level processing to break down the capital cost and manufacturing cycle time barriers. With M-Series, we leveraged our wafer-level manufacturing approach and added innovations in package structure, design methods and software, patterning technology, and inspection methodologies. M-Series will start production in 2013. Future product announcements will see our wafer-level processing capabilities applied to increasing levels of Si integration.

CSR: How do you see 2013 unfolding for the industry as a whole and for Deca? What is the company's strategy for future growth?

Demand for WLCSP and other forms of wafer-level interconnect will continue to grow at a healthy rate. Deca is positioned for strong growth in 2013. We will be focused on ramping production volume on our current WLCSP offering, as well as launching our M-Series into production.

BiTS Workshop Interconnectology Talk Show Features Deca's Tim Olson

There is a grass-roots initiative to introduce terminology that better defines processes used to build the next-generation of IC devices. "The term 'wafer-level packaging' is giving way to "electronic interconnect" as it's the interconnect technology that provides the value-add at the system level to packaging technologies," notes Tim Olson, CEO of Deca Technologies.

Olson will join fellow "interconnectologists," Scott Jewler, of ANSI, Simon McElrea, of Invensas, and semiconductor technology consultant, Ira Feldman, Feldman Associates, as guests on the'Talking Points' talk show on "Interconnectology" at BiTS 2013, March 4 at 1pm. The show is hosted by Queen of 3D, Françoise von Trapp, 3D InCites, and co-produced by Impress Labs.

Product News

Rudolph Unveils 2X Reduction Stepper Total Lithography System; Announces Azores Acquisition

Rudolph Technologies entered the back-end advanced packaging lithography market with the release of its JetStep™ Lithography System that features a 2X reduction stepper. The new system was developed in conjunction with the company's acquisition of Wilmington, Massachusetts-based Azores Corp. The product announcement and acquisition were announced by Rudolph in tandem. According to Rudolph, the company has combined its knowledge of advanced packaging and an established tool set for back-end manufacturing with Azores' proprietary technology and numerous features developed for the flat panel market into a solution that has not been utilized in the semiconductor market before.

The company further noted that the acquisition expands its business model and enlarges its role within the advanced packaging market. It is anticipated that the acquisition – one of several planned steps the company is taking to expand its portfolio – may result in more than doubling its total addressable back-end market. The terms of the deal were not disclosed, but the acquisition was an all cash transaction, utilizing less than 10% of the company's cash. It is expected that the new Lithography Systems Group (LSG) will account for approximately 10% of Rudolph's revenues in 2013, the first year of its manufacturing ramp. LSG is forecast to be accretive within its first year.

JetStep™ Lithography System

KLA-Tencor Launches ICOS® WI-2280 Wafer Inspector for LED and Adjacent Markets

KLA-Tencor Corporation has announced its next-generation light-emitting diode (LED) patterned wafer inspection tool, the ICOS WI-2280. Designed specifically for defect inspection and 2D metrology for LED applications, the ICOS WI-2280 also provides enhanced inspection capabilities and increased flexibility for microelectromechanical systems (MEMS) and semiconductor wafers spanning two inches to eight inches in size.

ICOS® WI-2280 Wafer Inspector

The ICOS WI-2280 represents the company's fourth generation LED wafer inspection system and it is built on its WI-22xx platform. The tool supports handling of whole wafers in carriers and diced wafers in hoop ring or film frame carriers to accommodate multiple media with minimal equipment changeover time. The WI-2280 also features an enhanced rule-based binning defect classification and recipe qualification engine, enabling manufacturers to achieve faster yield learning during production ramps, as well as improve process control and process tool monitoring strategies in their manufacturing process.

HITACHI Solder Paste Printers, Koh Young SPI Systems Interface for 'On-the-Fly' Print Process Optimization

Hitachi high-speed, high performance solder paste printers and Koh Young Technology's 3D Solder Paste Inspection (SPI) systems can now "talk" to one another via Koh Young's Closed Loop Interface process control software. The process control software brings the SPI system and the printer together via a closed-loop communications link to not only identify defects in solder paste printing, but correct them at the printer. This process optimization tool prevents soldering defects downstream that result in excess rework, productivity delays, and lower yields. Hitachi's HP-07 and HP-08 solder paste printers also have the capacity to accommodate large-size printed circuit boards with a range from 50 x 50 to 620 x 510mm.

Koh Young's aSPIre2 Solder Paste Inspection System.

Based on the true 3D measurements of the Koh Young SPI system (after the

print) communicated to the printer, the printer's software automatically adjusts printing parameters to optimize the print process and mitigate potential problems and defects. Whereas the SPI machine typically detects solder paste print defects and offers real-time defect analysis and trend charts, the KY Closed Loop Interface 'talks' to the printer, which automatically makes corrections. SPI print offset and theta measurements are sent directly to the printer for on-the-fly alignment correction. Automated offset corrections can be verified in real time through offset histograms and bull's-eye charts from KY SPC Plus software.

Multitest Announces MEMS Oscillator Capability for Its MT9928 Test Handler

Multitest announced that its equipment fully supports the advantages of MEMS oscillators. This capability is important because MEMS oscillators are considered to be a favorable alternative to the long-established, quartz crystal oscillator technology.

Besides the superior performance of MEMS oscillators, reliability and the more comprehensive features, one substantial advantage is that packaging and test of these devices is very similar to standard IC processes. Economy of scale can be achieved, which significantly contributes to the favorable cost structure, price and availability.

Test Handler MT9928

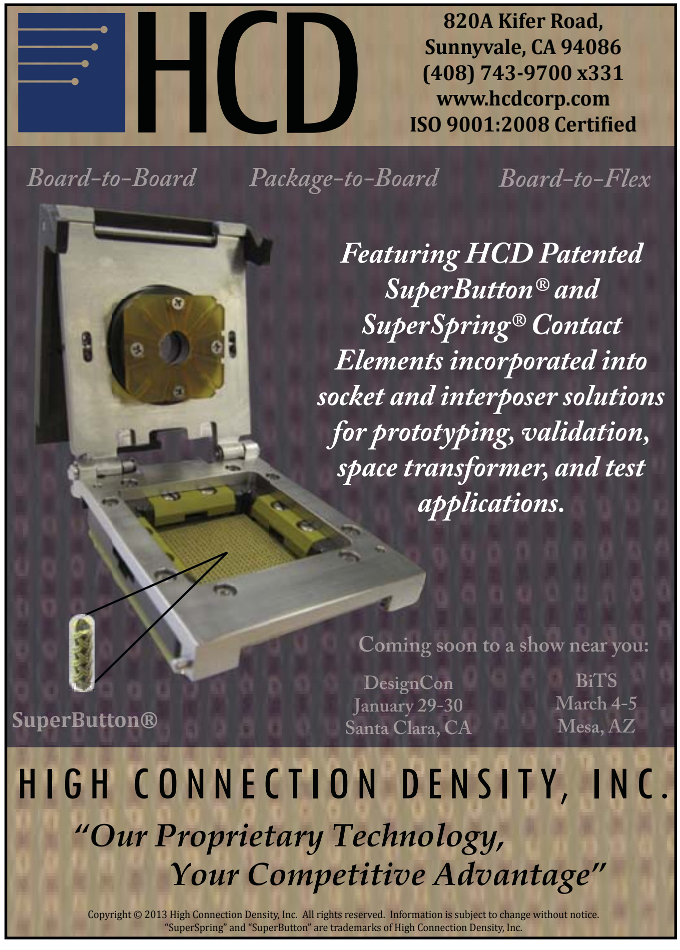
The company's standard Test Handler MT9928 has been deployed for calibrating and trimming MEMS oscillators at various customers. All systems were delivered as full plug and yield solutions, including the Multitest conversion kit, socket, and load board. All typical package sizes of MEMS oscillators are supported.

The MT9928 Gravity Feed Handler ensures the required temperature accuracy (up to +/-0.2K), but also provides high throughput and low cost of test, and as such, fully supports the favorable cost structure.

Imec Teams With Cadence to Present Automated Design-for-Test (DFT) Solution for 3D Memory-on-Logic

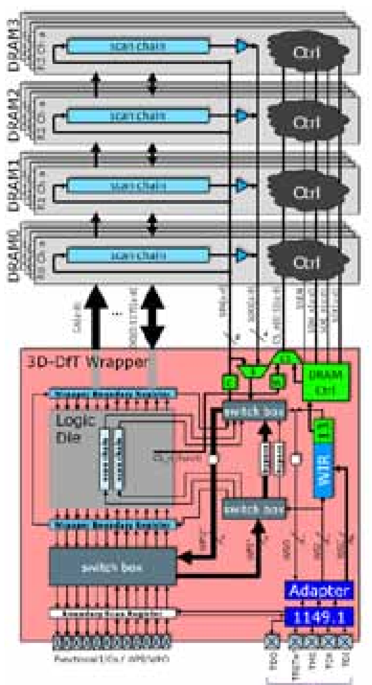
At the European 3D TSV Summit in Grenoble, France on January 22-23, 2013, imec, announced that, together with Cadence Design Systems, they have developed, implemented and validated an automated 3D Design-for-Test (DFT) solution to test logic-memory interconnects in DRAM-on-logic stacks. The solution, based on Cadence® Encounter® Test technology, was verified on an industrial test chip containing a logic die and a JEDEC-compliant Wide-I/O Mobile DRAM.

Memory-on-logic 3D stacks offer the possibility of heterogeneous integration with dense low-power inter-die interconnects. They are, therefore, among the first 3D products that will come on the market, enabling next-generation high-performance low-power mobile applications. Recently, JEDEC released a standard (JESD-229) for stackable Wide-I/O mobile dynamic random access memories (DRAMs) specifying the logic-memory interface. Unlike many previous DRAMs, the standard contains boundary scan features to facilitate interconnect testing. Imec and Cadence now present a design-for-test (DFT) architecture and corresponding automatic test pattern generation (ATPG) approach. It is an extension of their previously announced logic-on-logic 3D DFT architecture and it supports post-bond testing of the interconnects between the logic die and



the DRAM stacked on top of it.

The solution implemented by Cadence and imec includes the generation of DRAM test control signals in the logic die and the inclusion of the DRAM boundary scan registers in the serial and parallel test access mechanisms (TAMs) of the 3D test architecture. The automated design for test solution has been validated on an industrial test chip. The design of the test chip is an interposer-based 3D stacked IC which includes a silicon interposer base die, a 94mm^2 logic system-on-chip in 40nm technology, and a single Wide-I/O DRAM rank. The validation results show that the silicon area of the additional DFT wrapper is negligible compared to the total logic die size (<0.03%). Moreover, the test pattern generation was very efficient (tens of patterns, generated in only a few seconds) and effective (100% coverage of the targeted faults). All 3D-DFT logic in the logic die was automatically inserted with Cadence Encounter RTL Compiler while the Interconnect test patterns were generated with Encounter Test ATPG.

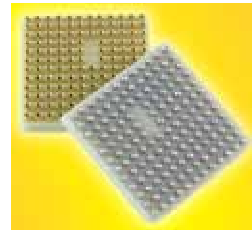


Imec's 3D wrapper extension for Wide-I/O DRAM

Part of the work has been performed in the project ESiP, which is co-funded by the ENIAC Joint Undertaking.

Ironwood's Newest BGA Socket Adapters Have Same Solder Ball Types as ICs Being Emulated

Ironwood Electronics' new high-performance socket – SF-BGA141A-B-32F –allows 1.27mm pitch, 15x15mm body, 12X12 array Linear's high efficiency switching mode buck-boost power supply IC to be placed in socket and operated without compromising performance in DC/DC applications. The Giga-snaP™ BGA socket adapter pair consists of SF-BGA141A-B-32F, patented female BGA sockets with machined pins epoxy over molded into an assembly that matches the male pin LS-BGA141A-31 adapter. The RoHS-compliant BGA socket is soldered to a PCB using standard soldering methods without warping. Both BGA socket and adapter are constructed with high-temperature FR-4 body assuring a match with target PCBs and preventing failures that occur because of CTE mismatch. The LS-BGA141A-31 BGA adapter, to which the user attaches a target 141 pin Linear power supply chip or other compatible chip, is plugged into the female BGA socket on the board. These new BGA socket adapters have the same solder ball types as the IC they are emulating and require half the force of conventional adapters at 5 pounds for the 141 pin device. The electrical path of the adapters is a high-priority performance issue with the physical length from the top connection point on the male adapter to the solder ball on the female socket being 4.5mm. This short connection length provides better transmission of high frequency signals. These adapters passed environmental tests (MIL-STD) and qualified for power supply applications. The Giga-snaP™ BGA socket adapter line is available in many different pin counts/pitches.



Giga-snaP™ BGA socket adapter pair

(continued from Page 39)

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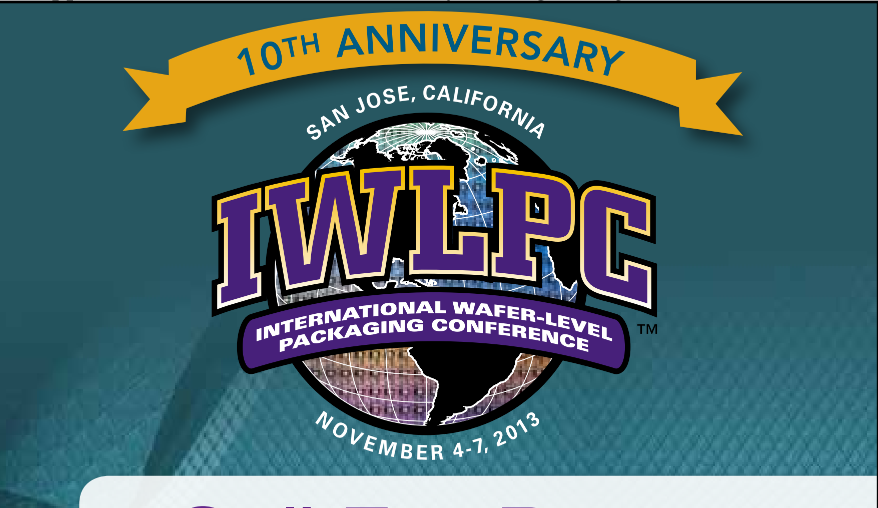
Biography

John H. Lau received his PhD degree from the U. of Illinois at Urbana-Champaign and is a Fellow at the Electronics & Optoelectronics Research Laboratory, Industrial Technology Research Institute (ITRI); email johnlau@itri.org.tw



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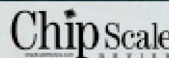

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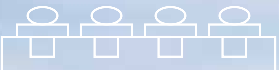

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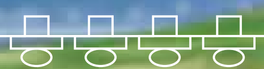

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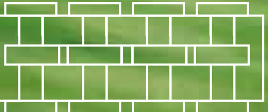

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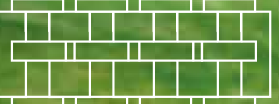

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