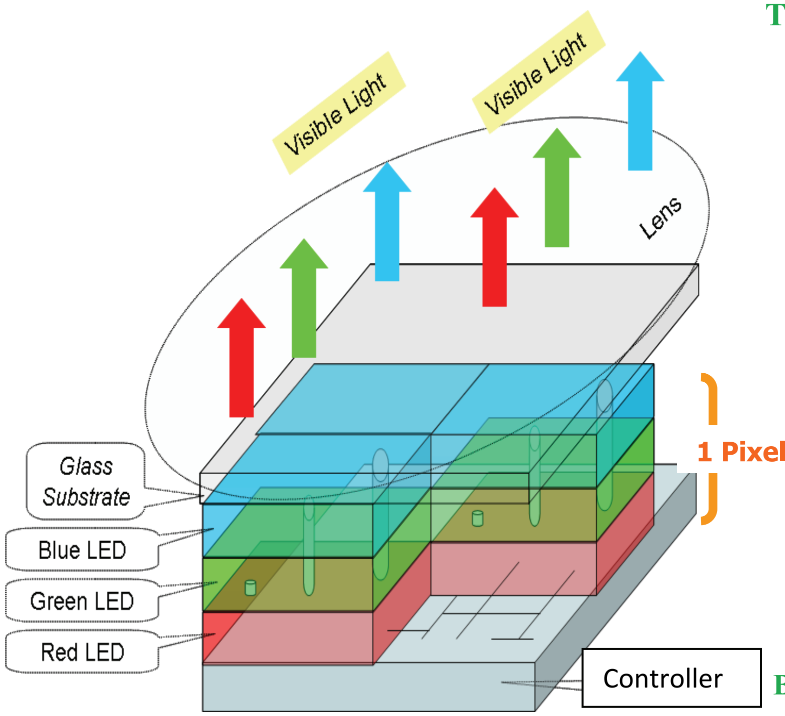
Technology Breakthrough

A Microdisplay with 1/10th the Power, 1cm^3 Volume, 10g Weight and Far Fewer Components



Technology:

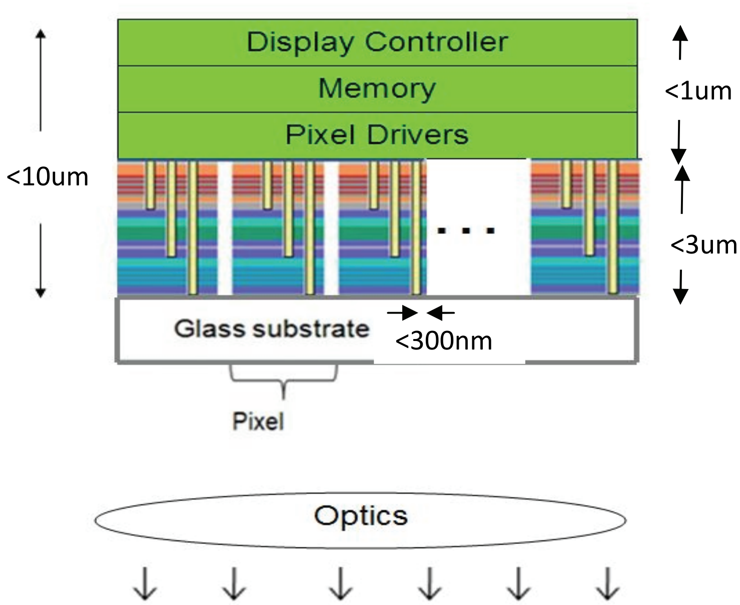
The monolithic 3D IC technology is extended by using a novel architecture with stacked RGB LEDs. This architecture avoids filters, polarizers and LCD layers when compared to today's displays. This, combined with efficient color-tunable RGB LEDs, provides an order of magnitude lower power consumption.

Key Features:

- Vertical interconnect pitch <300nm
- Thickness of stacked regions<10µm

See reverse side for more on monolithic 3D IC technology

1000x1000 Pixels Micro-Display ~ 1cm^2



Benefits:

- 8x-10x lower power consumption
- Dramatic reduction in cost since fewer components
- Display is constructed by dividing LED area into multiple pixels

Applications:

- Rugged heads-up displays
- Ultra-low power pico projectors
- Bright high-resolution hand held
- Mobile displays up to 10^6pixels/mm^2
- Flexible high bandwidth light pulse signaling
- Cockpit illumination
- Map lights

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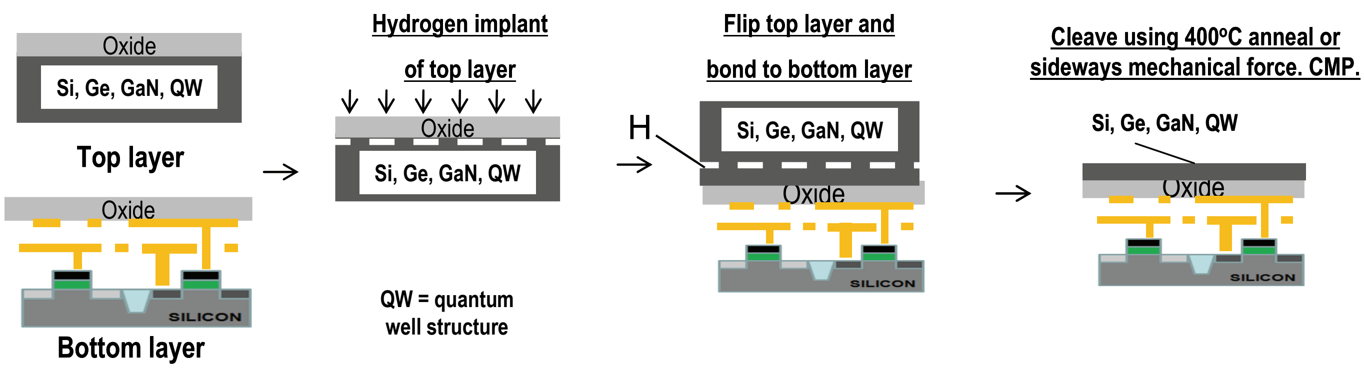
www.monolithic3d.com. •**Patents pending**

MonolithIC3D™ Technology Breakthrough

Layer Transfer Technology ("Ion-Cut")
Defect-free single crystal obtained @ <400°C

Leveraging a mature technology (wafer bonding and ion-cleaving) that has been the dominant SOI wafer production method for over two decades.

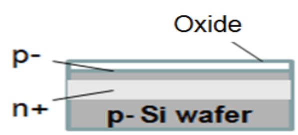
Innovate and create multiple thin (10s – 100s nanometer scale) layers of virtually defect free Silicon, Germanium, Gallium Nitride, and quantum well structures by utilizing low temperature (<400°C) bond and cleave techniques, and place on top of active transistor circuitry. Benefit from a rich layer-to-layer interconnection density.



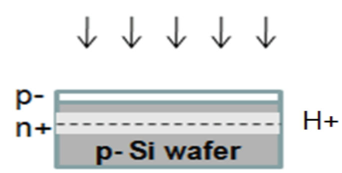
Create a layer of Recessed ChAnnel Transistors (RCATs), commonly used in DRAMs, by activating dopants at ~1000°C **before** wafer bonding to the CMOS substrate and cleaving, thereby leaving a very thin dopant stack layer from which transistors are completed, utilizing less than 400°C etch and deposition processes.

(a) Build transistors and interconnects for bottom wafer of 3D stack

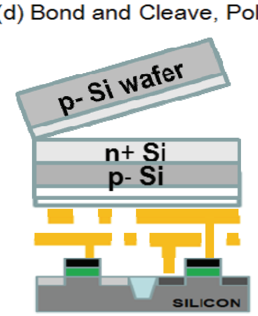
(b) Using new wafer, construct dopant regions and activate at ~1000°C



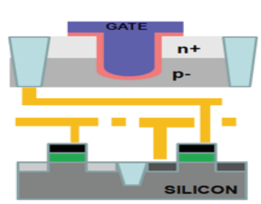
(c) Implant Hydrogen for Ion-Cut



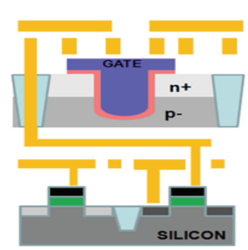
(d) Bond and Cleave, Polish



(e) Form RCATs using low temperature steps such as etch and deposition



(f) Thin Silicon layer enables well-aligned top layer features



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