

# Technology Breakthrough

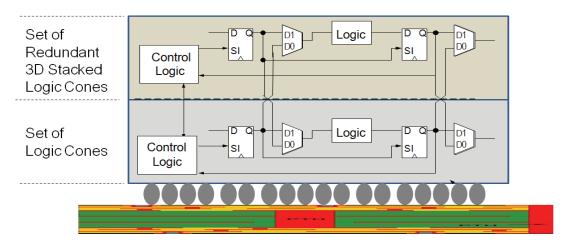
## Redundancy & Repair with Monolithic 3D



Technology: High-Yield Fault-Tolerant Systems with Monolithic 3D Integration

**Description:** Monolithic 3D has invented several techniques to obtain monolithic 3D integration with crystalline silicon transistors and copper wires at the most advanced lithography. Intelligent uses of 3D technology give reliable operation for systems with multiple logic and delay defects, and can provide a high tolerance for soft-errors and field repair. Consequently, monolithic 3D enables ultra large system integration previously thought unachievable because of yield issues.

## <u>Defect & Fault Tolerant Systems with 3D Technology</u>



### **Technology:**

- 3D Stacked Redundant Logic replaceable with logic-cone granularity
- Fault tolerant analog functionality, replaceable with module-by-module granularity
- Option for soft error tolerance and field repairs

#### **Benefits:**

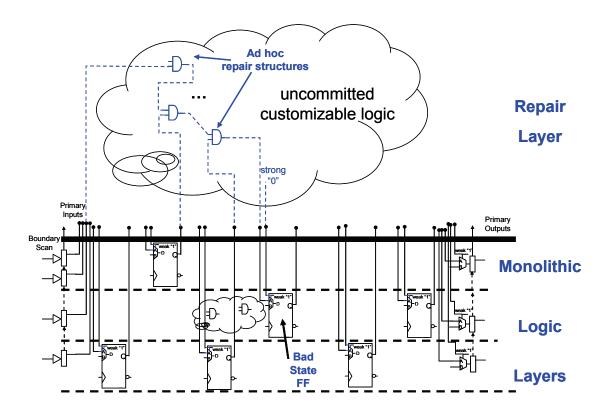
 Monolithic 3D integration with novel (patentpending) technologies. Connections between device layers are at minimum feature size.

- Redundant logic cone/block is directly above, imposing no performance penalty for redundancy scheme. Negligible design effort, since redundant layer is exact copy.
- Ultra-large scale integration, up to wafer scale integration, is possible without yield issues
  → invaluable for UAVs, packbots and other robotic applications.
- Can handle soft errors and other faults in the field. Useful for logic, analog and in general for any block. Intelligent use can reduce impact of variability in a chip.
- Due to additional cost for stacked silicon layer, particularly attractive when cost of chip is much smaller than cost of system, and where fault tolerance is important → military applications.



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## Repair & Yield Enhancement with 3D Technology



### **Technology:**

- Single Repair Layer on top of a stack of multiple monolithic silicon logic layers
- 3D Stacked Repair Layer made of Uncommitted Logic Gates
- Factory repair using direct-write e-Beam

### **Benefits:**

- Monolithic 3D integration with novel (patentpending) technologies. Connections between device layers are at minimum feature size
- Repair logic resides directly above defects, imposing no performance penalty for repair
- A single repair layer can repair multiple logic layers
- Enables high yield wafer-scale integration with current defect density
- Allows high yield ultra-large scale integration without TMR
- Allows selective replacement of slow paths
- Opens new frontiers for supercomputing and robotics