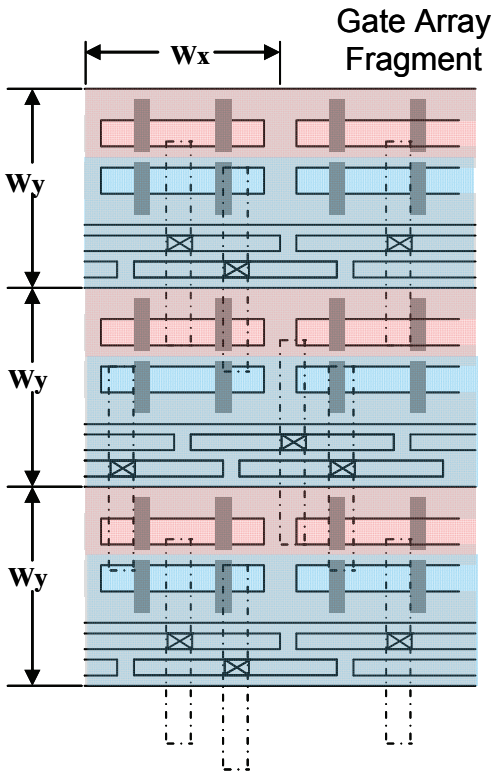
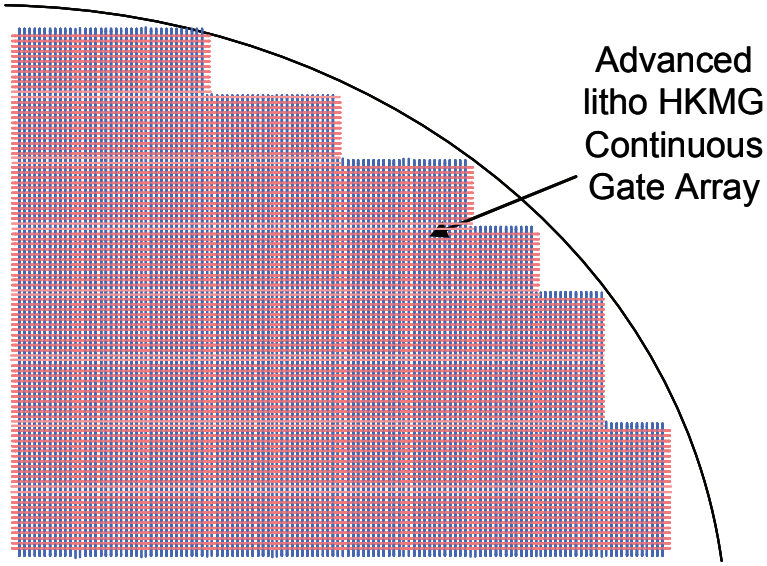
MonolithIC 3D™

Technology Breakthrough

Three-Dimensional Gate Array





Technology:

- **Dense High Performance HKMG Gate Array with continuous N/P strips**
- **Layer Transfer with Ion Cut for 3D stacking**
- **Gate Replacement after Ion Cut**
- **Alignment error guaranteed smaller than Wx and Wy independent of Layer Transfer**
- **Multiple stacking for ultra dense arrays**
- **Mix of GA and Memory wafers in stack**
- **Unidirectional layout**
- **Continuous Array style of wafer patterning**
- **Etching scribe lines per application demand**

Benefits:

- Very high density Gate Array terrain
- Easy patterning with unidirectional layout
- Continuous Array allows flexible dicing for variable-sized chips
- 3D stacking allows flexible ratio between memory and logic
- 3D stacking allows ultra-high device density
- Single mask set for a complete range of Gate Arrays

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www.monolithic3d.com. ◆ **Patents pending**

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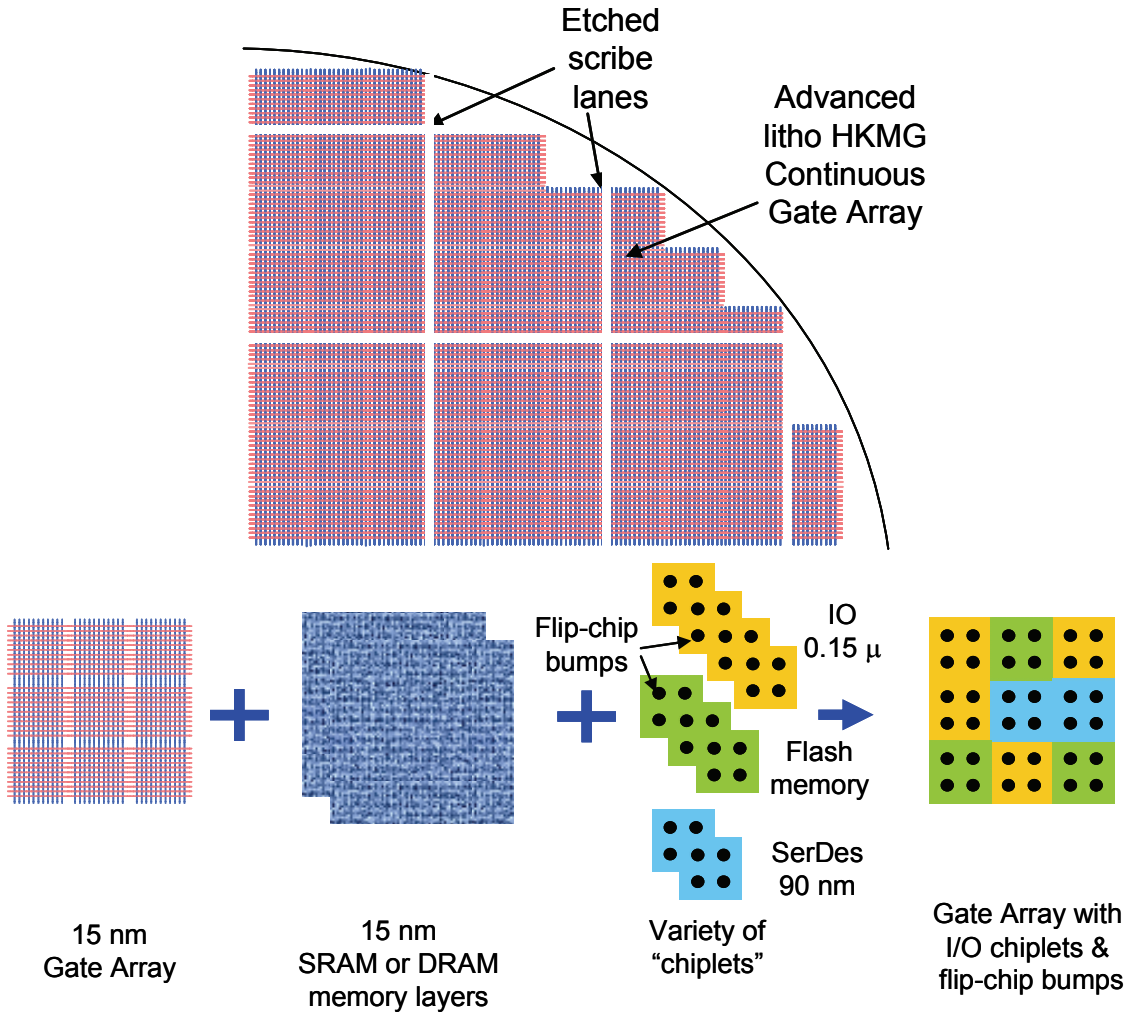
Inexpensive Arbitrary-sized Gate Array Manufacturing



Chip-on-Wafer I/O Chiplet Assembly

Technology:

- **Wafer-scale Continuous Array with custom-etched scribe lines**
- **Chiplets with I/O, analog functions, etc.**
- **Chiplets contain flip-chip bumping**
- **TSV or microbump-based Wafer-on-Wafer and Chip-on-Wafer 3D stacking**

Benefits:

- Arbitrary-sized Gate Array
- Flexible I/O and analog function configuration
- Possible re-use of older prequalified silicon I/O together with most advanced logic technology
- Gate Array family no longer needs costly multiple mask sets

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